

Atomic Vapor Deposition of complex high-k thin films for sub-90 nm CMOS devices

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Alternative high-k gate dielectrics and especially their processing methods become increasingly important to enable further CMOS scaling. For advanced CMOS and DRAM, a variety of industrial and research institutes are currently focusing their efforts in the field of alternative gate oxide replacements mainly based on HfO_2 and related silicates or aluminates ($\text{HfAl}_x\text{Si}_y\text{O}_z$). A lot of effort is currently dedicated to interface engineering aspects with a search for suitable production methods for the deposition process which meets standard CMOS requirements in terms of manufacturing cost and throughput. In this study, we provide an insight into a new deposition approach based on Atomic Vapor Deposition (AVD) which is specifically tailored for the interface-controlled growth of thin complex oxides - this at a high wafer throughput.

Atomic Vapor Deposition (AVD) is a unique MOCVD based deposition concept. This concept makes use of AIXTRON's TriJet[®] liquid precursor delivery system, which is equipped with 4 injection units - each independently controlled in injection frequency and opening time.

AVD is specifically tailored for the growth of complex oxides and metallic electrodes. Based on a pulsed injection of liquid precursors followed by a non-surface-contact evaporation, AVD was proven to enable interface controlled growth with atomic precision at high wafer throughput. By injecting small quantities of (diluted) liquid sources into a heated volume, precise precursor supply for the chemical reaction process can be obtained. The amount of injected liquid can be controlled in a very wide range by in-situ injecting frequency or digital valve opening time variation. According to this concept we demonstrated that AVD facilitates growth rates in the range of a few of $\text{\AA}/\text{min}$ up to 30

nm/min offering a wafer throughput larger than 20 wafers/h (Fig.1).

AVP proved to be an extremely promising deposition technique for the deposition of very thin HfO_2 layers on Si/SiO_2 wafers with an overall EOT of 16\AA (Fig.2). The permittivity value (k-value) observed in this study was in the range of 20, confirming a very low carbon content in the films.

Figures

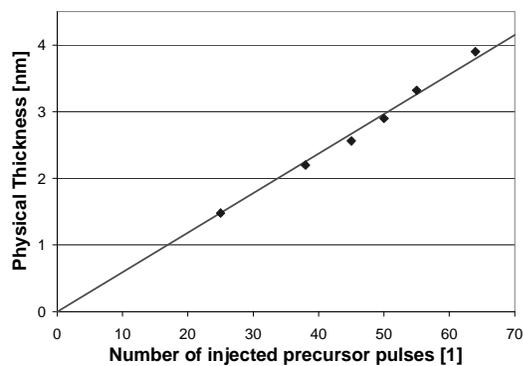


Figure 1. The film thickness for this study was found to be linearly dependent on the number of injected precursor pulses. The slope and in particular the value of the growth rate can be precisely controlled by in-situ pulse frequency control as well as by adjusting the molarity of the precursor solution, resulting in a high degree of film thickness controllability and reproducibility. The growth rate obtained can be tailored up to 25 nm/min , resulting in a wafer throughput in the order of 25-30 wafers/h in a single growth chamber.

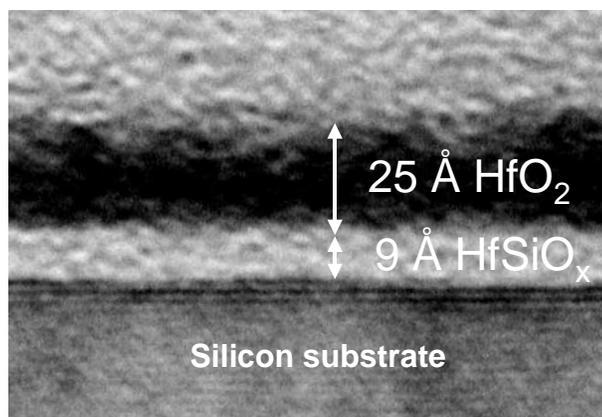


Figure2.

TEM pictures of HfO_2 layer deposited on a Si substrate subjected to a standard surface cleaning methods causing a remaining SiO_2 interface in the range of $7\text{-}8\text{\AA}$. Thus the initial SiO_2 interface increased just by $1\text{-}2\text{\AA}$ during the 550°C growth process. As far as electrical measurements on these samples are concerned EOT values obtained were as low as 16\AA .