FROM THE LAB TO THE FAB: TRANSISTORS TO INTEGRATED CIRCUITS

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Transistor action was experimentally observed by John Bardeen and Walter Brattain in n-type polycrystalline germanium on December 16, 1947 (and subsequently polycrystalline silicon) as a result of the judicious placement of gold-plated probe tips in nearby single crystal grains of the polycrystalline material (i.e., the point-contact semiconductor amplifier, often referred to as the point-contact transistor) [1-3]. The device configuration exploited the inversion layer as the channel through which most of the emitted (minority) carriers were presumed to be transported from the emitter to the collector. The point-contact transistor was manufactured for ten years starting in 1951 by the Western Electric Division of AT&T [4]. The *a priori* tuning of the point-contact transistor parameters, however, was not simple inasmuch as the device was dependent on the detailed surface structure and, therefore, very sensitive to humidity and temperature as well as exhibiting high noise levels. Accordingly, the devices differed significantly in their characteristics and electrical instabilities leading to "burnout" were not uncommon [5]. With the implementation of crystalline semiconductor materials in the early 1950s [3,6,7], however, p-n junction (bulk) transistors began replacing the point-contact transistor, silicon began replacing germanium [5,7] and the transfer of transistor technology from the lab to the fab accelerated.

We shall briefly review the historical route by which single crystalline materials were developed and the accompanying methodologies of bipolar transistor fabrication (i.e., grown junction, alloy and diffused). The oxide masking and photolithographic technique of Carl Frosch and Link Derick [8,9] and its embodiment in the mesa process, the utilization of the silicon oxide for the passivation of the silicon surface by Mohammed (John) Atalla and colleagues [10] and the development of the planar silicon transistor by Jean Hoerni (i.e., the planar process) [11-14] whereby the SiO_2 masking layer, utilized in the fabrication of diffused silicon transistors, was left in place for the passivation of p-n junctions intersecting the surface set the stage for MOSFET fabrication as well as a dielectric layer for supporting metallic conductor overlayers in the integrated circuit (IC) era.

The Si-SiO_2 diffusion technology, transferred from AT&T's Bell Telephone Laboratories (BTL) to Shockley Semiconductor to Fairchild Semiconductor Corporation and, hence, to the "Silicon Valley" led to the creation of the IC industry. The critical role of John Moll's laboratory at BTL in developing the oxidation, diffusion, lithography, aluminum metallization and thermocompression bonding for the fabrication of the junction transistors and silicon-controlled rectifier [15,16], in conjunction with Nick Holonyak [17], are reviewed.

The oxidation kinetics of silicon by Bruce Deal and Andy Grove [18], the explication of the charge and drift mechanisms in the Si-SiO_2 system by Deal et al. [19,20] and the role of Pieter Balk [21,22] in emphasizing the importance of post-deposition hydrogen and nitrogen annealing are briefly discussed. The mesa and planar processes described above paved the way for the fabrication of the IC by Jack Kilby [23-26] (utilizing the mesa methodology) and Bob Noyce [27-29] (utilizing the planar procedure) and the subsequent microprocessor era; the critical interconnection differences between the two patents are clarified by Walt Runyan and Ken Bean [30].

The early years of the IC from the 256 bit to the 1 M DRAM are then reviewed [31], building on Bob Dennard's one transistor cell structure [32] and associated scaling methodology [33-35]. Gordon Moore's remarkably prescient assessment that the number of memory bits would double per year (now taken as about 18 months), enshrined as Moore's law, became the productivity criterion by which the IC industry grew at about a 25% compound annual growth rate [36-39]. More than just monitoring productivity, whether by staying on the productivity curve or increasing manufacturing effectiveness, however, is required. Rather, modeling productivity—the identification of new productivity measures—is now required [40].

Finally, potential directions for enhanced IC performance, per the International Technology Roadmap for Semiconductors (ITRS) [41], are briefly discussed. These include both carrier transport mechanisms in the channel using variously strained structures to enhance the carrier mobility and new MOSFET device configurations, including various vertical transistor configurations [42].

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