LOGIC BASED EMBEDDED DRAM TECHNOLOGIES

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The main challenges of logic based embedded DRAM technologies including applications; process choices and trade-offs are discussed.

Embedded DRAM's (eDRAM) allow system designers to use high bandwidth, high performance and high-density memory to realize System On Chip (SOC). Embedded DRAM is therefore a powerful tool for ULSI if cost effective. Logic or stand-alone DRAM technologies have been used to realize eDRAM's [1-3]. Logic based technologies offer the advantage of high performance, and compatibility with existing standard cell libraries and cores, which is essential for SOC. The main challenge of logic based eDRAM is to find the right compromise between added process cost and memory density.

As far as applications are concerned, one of the main benefits of logic based eDRAM is higher performance. Some examples of high speed and high-resolution applications are graphics and networking, using wide bus width. Another benefit is cost reduction, if a system can be designed with fewer components: this applies to digital consumer applications like printers, cell phone and camcorders. In that case, cost analysis of added complexity versus memory density is key.

Process choices for logic-based eDRAMs are driven by 2 factors: compatibility with the logic transistor, and cost. For compatibility, the logic process has to remain unchanged in terms of spice parameters so that standard cell libraries and IPs can be directly usable. A typical choice is a 3-dimensional stacked DRAM cell with a hemispherical-grain polysilicon or MIM (Metal Interdielectric Metal) capacitor introduced in the logic interconnect by addition of high aspect ratio contacts (Fig.1-2). To maintain the compatibility with the logic process, low thermal budget recipes are mandatory to build the capacitor: low temperature nitrides or colder solutions using MIM with high K dielectrics. For low cost requirements, CUB (Capacitor Under Bitline) is the preferred choice to minimize the number of added masks, using the first interconnect level as bitline. Moreover to reduce the added steps to the logic process, the cell transistor remains silicided, with abrupt junctions. Retention time is not considered as a critical factor as long as design solutions allow the implementation of hidden refresh and ECC (Error Correction Code) to improve the DRAM robustness.

For trade-offs between process cost and DRAM density, the stacked capacitor lies between 2 other architecture choices: planar cells and deep trench cells. The planar cell allows a very easy integration with only one added mask, but cell sizes remain 2 to 3 times larger than stacked or trench cells, restricting the use to small DRAM capacity. On the other side the trench cell is very competitive in terms of size, allowing high memory density, but with added process complexity, close to a stand-alone DRAM process.

Logic based embedded DRAM technologies have been proven beneficial for SOC (Fig.3), when the right trade-offs between performance and cost savings are achieved.

[1] H.Ishiuchi et al., IEDM Tech. Digest, p.33, 1997
[2] M.Yoshida et al., IEDM Tech. Digest, p.41, 1999
[3] M.Hamada et al., IEDM Tech. Digest, p.45, 1999

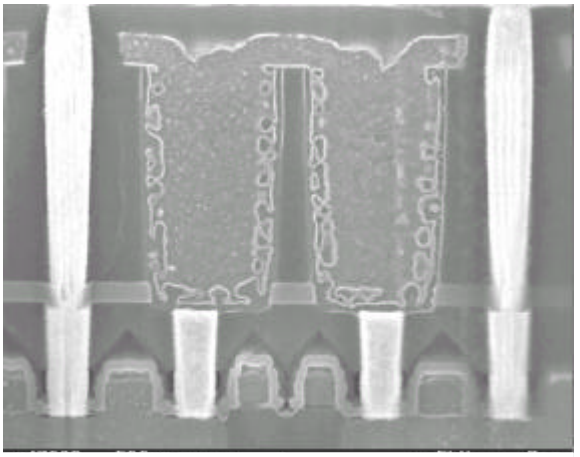

Fig. 1 : SEM Cross Section of a stacked CUB DRAM cell in 0.13 µm Technology

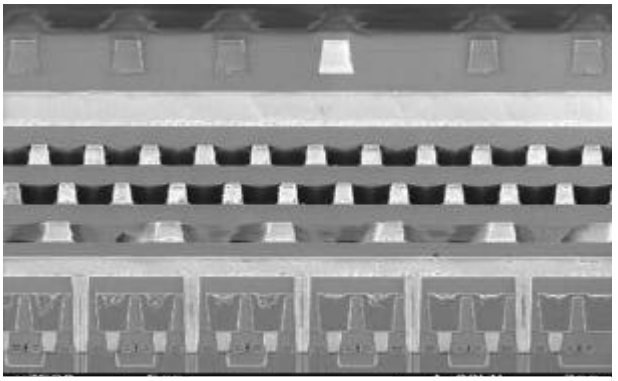

Fig. 2 : SEM Cross Section of a logic-based eDRAM process with 6 metal levels.

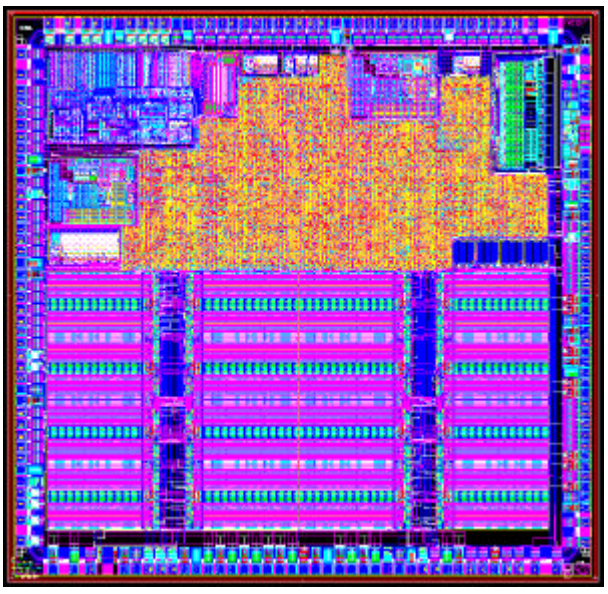

Fig. 3 : Typical example of eDRAM circuit for printer application