Single-Wafer Technology in a 300-mm Wafer Fab

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The trends in semiconductor manufacturing are using larger silicon wafers to reduce the cost and single-wafer processing to reduce wafer-to-wafer process variability and cycle time [1][2][3][4][5].

One of the examples we developed for single wafer processing is wet clean system [6]. Agents are added to SC1 and SC2 solutions to increase etching ratio and enhance cleaning efficiency. That reduces etching time one tenth of conventional batch clean even in room temperature as shown in Fig. 1. Throughout our 300mm process development work, we were aware that process time reduction sometimes results in a loss of film uniformity in CVD processes. So, one of our priorities was to achieve good film uniformity simultaneously with shorter process times. With the optimized process, good uniformity were achieved with a RT CVD system. A high temperature single-wafer oxide system was introduced to replace the conventional batch oxidation for gate oxide. Higher temperature oxidation is known to provide higher activation energy, which makes shorter process times possible and results in defect-free oxidation and better surface roughness. As shown in Fig. 2, RT oxide showed better Gm and Qbd characteristics compared with furnace oxidation. All of the long time anneal processes are replaced by RTA to reduce cycle time. Densification anneal for STI filling oxide, that is around 1000 degree C for 10-20 minutes in a conventional batch process, is replaced to RT anneal at 1000 degree C for 20 seconds without recesses or voids. The key is to optimize liner oxide condition and using HDP oxide.

One potential drawback to a single-wafer process might be higher sensitivity to plasma damage. Backside films electrically float the wafer during plasma processing and reduce plasma damage. However, no films are deposited on the backside of the wafer in single-wafer processes. All plasma processes -- dry etching, other plasma CVD, sputter, and ashing -- are carefully optimized to eliminate plasma damage.

Engineering Data analysis is effective to detect parametric defects and enhance yield quickly [7]. We implemented Chamber sensitivity analysis to find out particular chambers cause yield loss or large process variability. That is very effective to enhance the yield quickly in single-wafer processing (Fig.3).

Fully integrated 0.18 um technology with an all single-wafer process in a 300-mm wafer fab provides drastic cycle time reduction. As the results, a very aggressive cycle time (0.25 days per layer) with high yield and excellent reliability in double polysilicon 0.18um LOGIC process has been demonstrated.

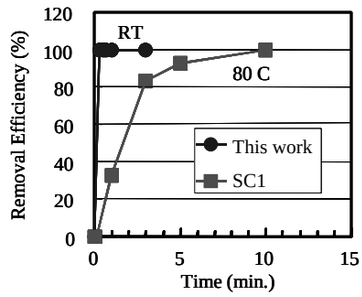

Fig. 1 Short time particle removing with the new solution

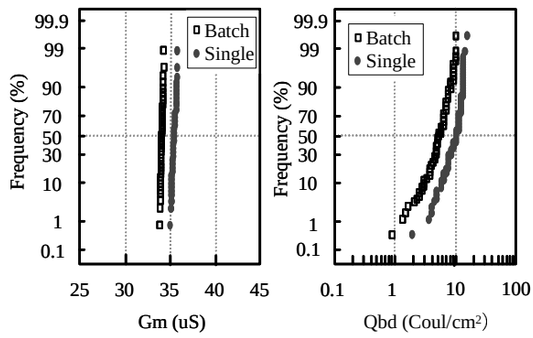

Fig. 2 Gm and Qbd comparison between Batch and Single-wafer processing

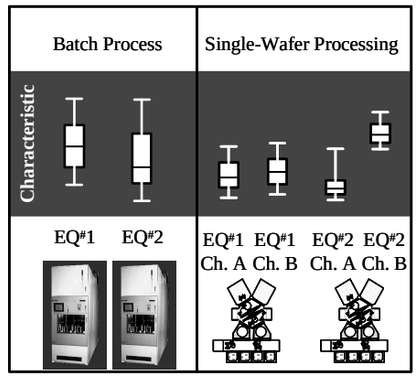

Fig. 3 Effectiveness of Chamber sensitivity analysis

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