The Impact of Single Wafer Processing on Process Integration

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Abstract

A study of annual semiconductor sales growth between 1995 and 2001 shows negative sales growth in year 1996, 1998, and 2001 [1]. Between 2002 and 2006, the next dip is expected to come in 2005[1]. Thus, the boom-bust cyclic nature of the semiconductor industry is expected to continue at least in the near future [1]. In order to continue manufacturing low-cost semiconductor products with improved performance, reliability and functionality, manufacturing beyond 70 nm nodes poses many new process integration challenges. The key new challenges include introduction of new materials, introduction of new processes, reduced time to market, new products and overall cost reduction [2]. Some of the notable key new material and process challenges include the introduction of silicon on insulator (SOI) wafers in main stream production, inventing a new gate/high-κ dielectric process and inventing a new contact technology yielding very low resistance per unit width i.e., < 100 Ω/μ [3]. For technology nodes below 70 nm, the fully depleted SOI structures will require 10-20 nm thick ultra thin silicon films across the 300 mm diameter wafers [4]. Any fluctuation in silicon film thickness will degrade the circuit performance and will not permit the use of SOI wafers in mainstream production.

The current mega fabs are dominated by batch processing. In future, batch processing will play a reduced role in mega fabs. The agile manufacturing based on mini fabs will be driven by shorter products life and dominated by single wafer processing (SWP). In a recent publication [5], we have shown that for manufacturing beyond 70-nm node, we expect the dominance of SWP. In the ultimate limit of IC manufacturing, the SWP will take over batch processing.

In this paper we will describe the importance of SWP in process integration. In addition to fundamental issues, several examples will be given that demonstrates the superiority of SWP on batch processing. As an example, using SWP based rapid thermal processing assisted atomic layer deposition system we have got excellent results of high-dielectric constant materials. For a 2.4 nm ZrO_2 film, the leakage current density of 1.83×10^{-11} A/cm^2 and capacitance per unit area of 8.17 μF/cm^2 were measured. These results show significant improvement of leakage and capacitance characteristics over other high κ materials reported in the literature.

References:

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