ADVANCED MULTILEVEL INTERCONNECTS TECHNOLOGIES FOR 40- nm Lg DEVICES

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Abstract

10 level Cu interconnects have been developed for 90 nm high speed processing logic devices operating in the above 3 GHz band. The fully integrated Cu Damascene process provides a high enough capability for production and it is shown that the use of Cu/SiLK™ (k = 2.65) and Cu/SiOC (k = 3.1, CORAL™) in Cu/VLK satisfies the requirements of RC design and reliability. Wiring capacity is below 190 fF/mm at the minimum feature size of 280 nm line and space in Cu/SiLK™ interconnects which yields the lowest effective k-value (k_{eff}) of 3.0. An adequate reliability in terms of Electro-Migration (EM), Stress Migration (SM), and packaging resistance has been demonstrated.

This paper described production-worthy Cu/VLK multi-level interconnects for 90 nm interconnect technology. A roadmap towards 65 nm and beyond will be presented.

90 nm Cu Damascene Process and Features

Cu Damascene interconnect is formed on ultra-high-density 6T SRAM with a minimum cell size below 1 μm^2 and 40 nm gate length, with 960 µA/µm and 300 µA/µm of an NMOS on-current and off-current at 1V, respectively [1]. In this transistor, a 320 psec access time (1.7 times faster than 130 nm technology) at above 3GHz has been achieved for a 144-kb SRAM macro [2].

The 10 interconnect levels are integrated using a Dual-damascene (DD) process as shown in Figure 1. A lot of expertise has been accumulated for Cu Damascene technology since the 180 nm process at Fujitsu [3]-[8]. Different dielectric materials are used at different levels in the structure, i.e. levels M1-M4 (280 nm pitch) use SiLK™, M5-M8 (560 nm pitch) use Silicon-Oxy-Carbide (SiOC, CORAL™), and M9-M10 (840 nm pitch) use SiO_2. ArF lithography with an Optical Proximity Correction (OPC) technique is used for patterning of minimum features.

Electrochemical Cu Deposition (ECD) is performed on a sputtered Cu/Ta bilayer, with the Cu and Ta being used as a seed layer and Cu diffusion barrier, respectively. A continuous Ta layer of the order of 8 nm in thickness is used at the sidewall of via-holes to prevent agglomeration of seed Cu and void-formation in the ECD-Cu. Since the presence of micro-voids with typical sizes below 5 nm due to plating chemistry, and random grains degrade the reliability of the Cu interconnect, an optimized ECD-Cu process involving control of the additive concentration and plating rate, and annealing (<200°C) to recrystallize the metallurgically meta-stable film is used

Electrical Characteristics and Reliability

Wiring capacitance below 190 fF/mm is low enough for the requirements of RC delay design and lower than that of 130 nm technology using SiLK™/SiO_2 hybrid structure. This is because SiC (k = 4.5) is used instead of SiN (k = 7) as a cap layer of hybrid structure, and SiLK™ is used between the vias without SiO_2. As a result, the lowest k_{eff} of 3.0 at a narrow line and space has been achieved.

Figure 2 shows life time due to Electro-Migration (EM) failure compared to 130 nm technology for a stress condition of 250°C and 2.5 MA/cm^2. Similar reliabilities are seen even for different dielectric structures (SiLK™/SiO_2 hybrid vs. SiLK™) and smaller feature size. Figures 3 shows the resistance change of via-chains for Cu/SiLK™. Samples are thermally stressed at 200°C for 504 hours and Stress Migration (SM) failure is evaluated. No significant resistance changes are observed for Cu lines ranging in width from 0.14 µm to 3 µm.

For packaging reliability, even in case of the smallest feature size in the Cu/SiLK™ multi-level interconnects, a 100% yield is obtained after 1000 thermal stress cycles from –65°C to 150°C. Accordingly, these Cu technologies promise production-worthy reliability from wafer process to packaging and can be used for the highest performance microprocessors in 90 nm node.

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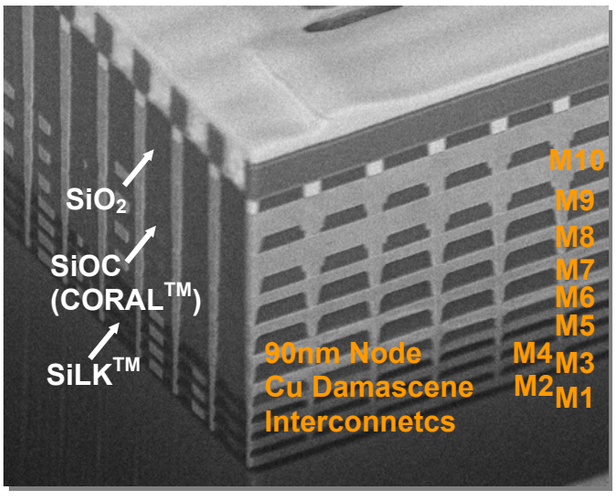

Fig. 1. 3D view of the 10 level Cu Damascene interconnects.

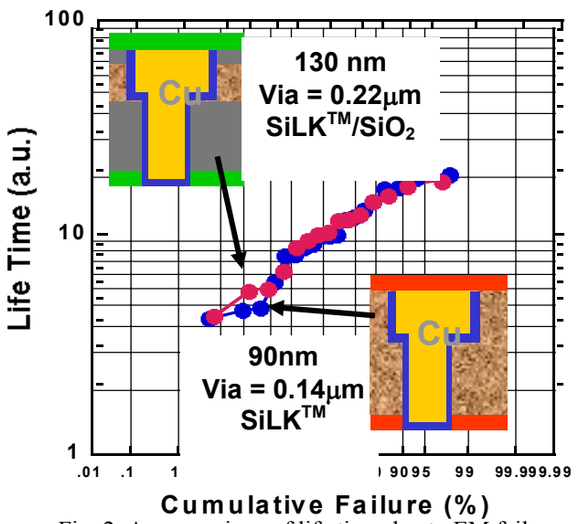

Fig. 2. A comparison of life time due to EM failure.

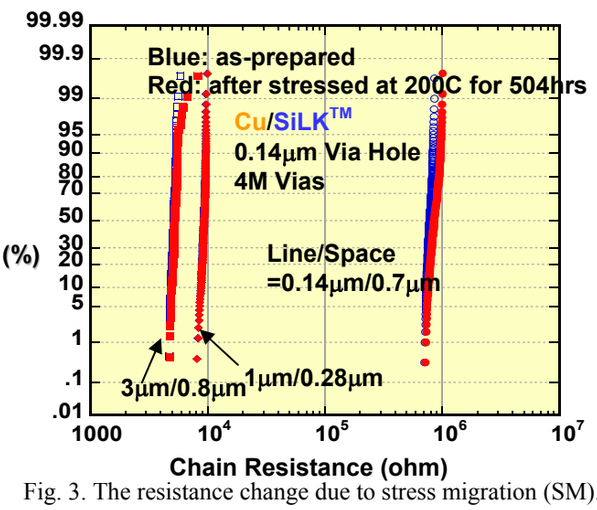

Fig. 3. The resistance change due to stress migration (SM).