Performance Limitations of Metal Interconnects and Possible Alternatives

Krishna Saraswat, Pawan Kapur and Shukri Souri
Department of Electrical Engineering,
Stanford University, Stanford, CA 94305, USA

Continuous scaling of VLSI circuits can pose significant problems for interconnects, especially for those responsible for long distance communication on a high performance chip. Both power and delay of these interconnects is likely to rise significantly in the future. International Technology Roadmap for Semiconductors (ITRS) predicts, that in spite of new materials like Cu and low-k dielectric, beyond the 130nm technology node, performance improvement of advanced VLSI is likely to begin to saturate unless a paradigm shift from present IC architecture is introduced. Our modeling predicts that the situation is worse than anticipated in the ITRS, which assumes that the resistivity of copper will not change appreciably with scaling in the future. We show that resistance of interconnect wires in light of scaling induced increase in electron surface scattering, fractional cross section area occupied by the high resistivity barrier and realistic interconnect operation temperature will lead to a significant rise in the effective resistivity of Cu [1]. Although, above constraints have been insignificant in the past, they are beginning to effect the interconnect performance and will become increasingly important with the aggressive scaling suggested in the ITRS [2]. In the light of various metal interconnect limitations, alternate solutions both at technology and architectural level need to be pursued.

One such promising technique is 3-D ICs with multiple active Si layers [3]. A large number of information signals paths could be transferred from horizontal interconnects to vertical interconnects. This can potentially increase transistor packing density, reduce chip area, interconnect length and therefore interconnect delay. Our simulations show that vertical integration of devices would allow a substantial reduction in chip size and thus limiting the maximum required interconnect wire length resulting in reduced interconnect delay. Presently, there are several possible fabrication technologies being investigated that can be used to realize multiple layers of active-area separated by inter-layer dielectrics (ILD) for 3-D circuit processing. These include epitaxial growth of a single crystal Si seeded from an open window in the ILD on Si substrate [4], bond two fully processed wafers [5] on which devices and interconnects are fabricated on the surface and solid phase crystallization using seeding agents such as Ni [6].

Another promising technique is optical interconnects with potential advantages in bandwidth, delay, cross-talk and power. While, the usefulness of optics in chip to chip communication is becoming clearer, there exists a considerable ambiguity in utility of optical interconnects in high performance on-chip applications. We have modeled the optical interconnect system delay, bandwidth and power consumption and compared the performance between electrical and optical interconnects [7]. There exists a critical length well within the chip size, beyond which the optical system is faster than the fastest copper system with repeaters. There is quite a bit of doubt as to the adequacy of conventional metal based clock distribution schemes to meet performance specifications in the future. Therefore, one of the first application of optical interconnects on-chip is believed to be in clock distribution because of reduction in skew and jitter and in some cases even power advantages. The optical system consists of the transmitter (laser), the medium (waveguide) and the receiver. Integration of optical clocks could be done by placing transmitter off chip, using free space as the transmission medium and the receiver including a detector on the chip. Ge appears to be a very attractive choice for this purpose. Ge has a higher low-field carrier mobility which should allow the fabrication of high performance deep sub-micron Ge MOSFETs. In addition, the smaller optical bandgap of Ge broadens the absorption wavelength spectrum allowing opto-electronic integration to enhance CMOS functionality. Unlike Si, however, the lack of a stable native oxide hinders the passivation of Ge surfaces. Recently we have demonstrated MOS devices on Ge with ZrO_2 gate dielectric [8]. With more development, this novel technology should allow the heterogeneous integration of high performance deep sub-micron Ge MOSFETs and optical detectors on Si.

Acknowledgments: The authors would like to acknowledge the DARPA HGI program and the MARCO Interconnect Focus Center for supporting this work.

References

[1]. P. Kapur and K. C. Saraswat “Comparisons Between Electrical and Optical Interconnects for On-Chip Signaling,” Proc. IEEE Int. Interconnect Tech. Conf., June 2002, San Francisco, pp. 89-91.

[2]. P. Kapur and K. C. Saraswat “Power Dissipation in Optical Clock Distribution Network for High Performance ICs,” Proc. IEEE Int. Interconnect Tech. Conf., June 2002, San Francisco, pp. 151-153.

[3]. K. Banerjee, S. J. Souri, P. Kapur and K. C. Saraswat, "3-D ICs: A Novel Chip Design for Improving Deep Submicron Interconnect Performance and Systems-on-Chip Integration,” Proc. IEEE, Vol. 89, No. 5, May 2001, pp. 602-633.

[4]. G. W. Neudeck, S. Pae, J. P. Denton, and T. Su, “Multiple layers of silicon-on-insulator for nanostructure devices,” *J. Vac. Sci. Technol. B* 17(3), pp. 994-998, 1999.

[5]. Fan, A. Rahman, and R. Reif, “Copper wafer bonding,” *Electrochemical and Solid State Letters*, vol. 2(10), pp. 534-536, 1999.

[6]. S. Y. Yoon, et al., “A high-performance polycrystalline silicon thin-film transistor using metal-induced crystallization with Ni solution,” *Jpn. J. Appl. Phys., Part 1*, pp. 7193-7197, Dec. 1998.

[7]. P. Kapur and K. C. Saraswat “Comparisons Between Electrical and Optical Interconnects for On-Chip Signaling,” Proc. IEEE Int. Interconnect Tech. Conf., June 2002, San Francisco, pp. 89-91.

[8]. C. O. Chui, S. Ramanathan, B. Triplett, P. McIntyre, and K. C. Saraswat, “Germanium MOS capacitors incorporating ultrathin high-□ gate dielectric,” *IEEE Electron Device Lett.*, vol. 23, pp. 473-475, Aug. 2002.