

## Applications of Silicon Germanium Electrodes in VLSI

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### INTRODUCTION

Because device scaling has been challenged by numerous difficulties, there has been significant interest in recent years to use silicon germanium ( $\text{Si}_x\text{Ge}_{1-x}$ ) in ULSI technology.<sup>(1)</sup> This article summarizes the ULSI applications of  $\text{Si}_x\text{Ge}_{1-x}$  material as electrodes in MOSFET gates, in contact landing pad, and in capacitor electrodes.<sup>(2, 3)</sup> Challenges of  $\text{Si}_x\text{Ge}_{1-x}$  material for future generation devices are presented and possible technology directions are also discussed.

### EXPERIMENTS

CMOS is fabricated with nitridized  $\text{SiO}_2$  gate dielectrics with polysilicon and/or  $\text{Si}_x\text{Ge}_{1-x}$  gate electrodes. Typical LDD and S/D implants, with thermal cycles that include RTP and furnace annealing, are used for doping. Transistor characteristics and quasi-static C-V are measured on these devices to compare the polysilicon gate and poly  $\text{Si}_x\text{Ge}_{1-x}$  gate electrodes.

Polysilicon and  $\text{Si}_x\text{Ge}_{1-x}$  films are deposited onto a 1000Å thick thermal oxide layer. Various doping species are implanted into them and activated by RTA. Sheet resistance is measured for both polysilicon and  $\text{Si}_x\text{Ge}_{1-x}$  films. Polysilicon and  $\text{Si}_x\text{Ge}_{1-x}$  are also deposited into typical contact strings that are formed onto active area through ILD and connected by metal lines. Contact resistance is measured after the thermal cycles, including RTP and furnace anneals.

Stacked capacitors are formed using hemispherical grain (HSG) bottom electrode via seeding and anneal amorphous silicon and  $\text{Si}_x\text{Ge}_{1-x}$  layers. Typical ONO dielectrics are used; polysilicon and  $\text{Si}_x\text{Ge}_{1-x}$  are used for top electrodes. After thermal activation, C-V and I-V are measured for the capacitor characterizations.

### RESULTS

Figure 1 shows the valence and conduction band changes in  $\text{Si}_x\text{Ge}_{1-x}$  gate electrodes relative to the polysilicon gate electrode. Both conduction and valence bands are lowered with the  $\text{Si}_x\text{Ge}_{1-x}$ . The valence band is lowered more than the conduction band. Earlier work indicates that the conduction band of pure Ge material is in the range of 50mV lower than Si and that the valence band is approximately 400mV lower than Si.

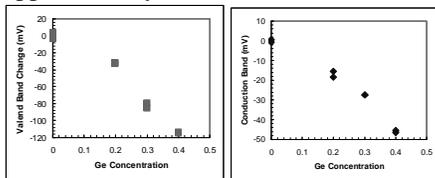


Figure 1. Energy band shifts of  $\text{Si}_x\text{Ge}_{1-x}$  gate.

Figure 2 shows the CMOS transistor drive current ( $I_D$ ) versus sub-threshold voltage ( $SV_T$ ) of the polysilicon and  $\text{Si}_{0.8}\text{Ge}_{0.2}$  gate. The Poly  $\text{Si}_{0.8}\text{Ge}_{0.2}$  gate improves on the polysilicon gate for the PMOS transistor. However, the NMOS transistor shows reverse behavior. The same is true for high Ge concentrations.

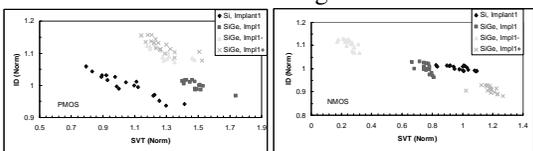


Figure 2. CMOS  $I_D$  vs.  $SV_T$  with polysilicon and  $\text{Si}_x\text{Ge}_{1-x}$  gate.

Figure 3 shows the resistivity of 850Å polysilicon and  $\text{Si}_x\text{Ge}_{1-x}$  films implanted with N- and P-type dopants after annealing by RTA.  $\text{Si}_x\text{Ge}_{1-x}$  implanted with boron results in lower resistivity than Si. Yet with As and P implants, the resistivity of Si is lower than  $\text{Si}_x\text{Ge}_{1-x}$ .

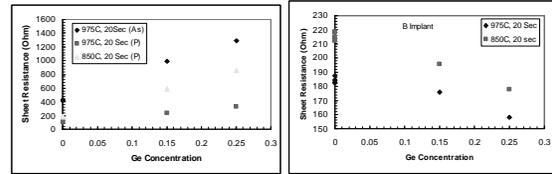


Figure 3. Resistivity of both N and P-type dopants in Polysilicon and  $\text{Si}_x\text{Ge}_{1-x}$ .

Figure 4 shows the N-type contact (two different kinds) string resistance measured over polysilicon and  $\text{Si}_{0.9}\text{Ge}_{0.1}$ .  $\text{Si}_{0.9}\text{Ge}_{0.1}$  shows higher resistance than Si. This increase in contact resistance will impact the transistor performance if the polysilicon contact landing pads are used.

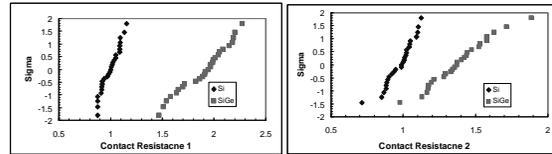


Figure 4. Contact resistance for poly Si and SiGe.

Figure 5 shows SEM pictures of HSG formed by seeding and annealing as-deposited amorphous Si and  $\text{Si}_x\text{Ge}_{1-x}$  films. Figure 6 shows the corresponding capacitance at various applied voltage for the capacitors fabricated with HSG electrodes.

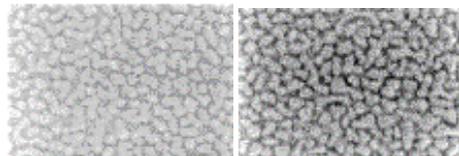


Figure 5. HSG formed on Si (left) and SiGe (right).

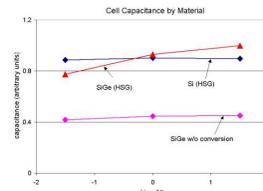


Figure 6. C-V characteristics for both Si and SiGe HSG bottom electrode.

### CONCLUSIONS

$\text{Si}_x\text{Ge}_{1-x}$  material offers attractive electrical properties to enhance device performance. Future ULSI devices can benefit from the  $\text{Si}_x\text{Ge}_{1-x}$  electrodes. However, integration challenges do persist for this material in various applications due to its material properties. The use of the  $\text{Si}_x\text{Ge}_{1-x}$  material in the manufacturing environment poses another challenge.

### ACKNOWLEDGEMENTS

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### REFERENCES

1. David L. Harame et al., *IEEE Trans. Electron Devices*, **48**, 2575 (2001).
2. C. H. Chen et al., *Solid-State Electronics*, **46**, 597 (2002).
3. Sung-Kwan Kang et al., "Gate Stack and Silicide Issues in Silicon Processing," *MRS Proceedings*, **C7.1.1-C7.1.6**, 611 (2001).