Ultra-shallow Junction Formation by Low Energy Ion Implantation and Flash Lamp Annealing.

Kyoichi Suguro, Takayuki Ito, Takaharu Itani, and Toshihiko Iinuma

Process & Manufacturing Eng., Semiconductor Company,

TOSHIBA Corporation, Yokohama , Japan

8, Shinsugita-cho, Isogo-ku, Yokohama235-8522, Japan

E-MAIL:suguro@amc.Toshiba.co.jp

Ultra shallow junction with low resistance is required to improve short channel effects and reduce parasitic resistance in 45-65nm technology node. Since the gate length for high performance MOSFETs shrinks to 20-30nm, the extension depth (pn junction depth near the gate edge) is required to be shallower than 20nm. However, current RTA tool is confronted with the trade-off problems of thermal diffusion of dopant atoms and electrical activation, which is limited by solid solubility of impurity atoms. Therefore, RTA is required to suppress impurity diffusion while keeping the electrical activity. In this viewpoint, higher temperature and shorter annealing time are desirable. RTA is also required to reduce dislocation density so that the pn junction leakage specification of high performance MOSFETs should be satisfied.

In order to minimize the annealing time at high temperatures, we investigated various rapid thermal annealing methods and have developed flash lamp annealing (FLA) technology [1]. Similar flash lamp annealing is reported in the literature. [2-3] However, there is an important issue on FLA technology. Ultra-short time heating sometimes causes slip defects and cracks in wafers, and the breakdown (explosion) of wafers in the worst case. The suppression of wafer damage is most important issue in ultra-short time annealing. The main cause of the wafer damage such as slip or crack generation in a Si substrate is the strain generated during ultra-rapid heating in 1 msec by flash lamps. By optimizing the substrate pre-heating and radiation energy as well as hardware configuration, we succeeded in obtaining both lower sheet resistivity and shallower junction depth.[4-5] In this paper, we review and discuss the ultra-shallow junction technology by using ultra-low energy ion implantation and improved FLA.

In spike RTA, the time length above 900 degree C is 2-3 sec, however, in FLA the heating time is only 1msec. FLA apparatus is consisted of Xe flash lamps in upper side of a 8 inch Si wafer and the wafer is put on the hot plate, which is used in assist heating of the wafer. Luminescence spectrum of Xe flash lamp is white light. The assist heating temperature was set at 200-500 degree C by the hot plate for several 10 sec and Xe flash was irradiated for about 1 ms pulse.

SIMS analysis clarified that the boron diffusion was suppressed and 14nm junction depth defined at $1E18cm^{-3}$ was successfully obtained by BF_2 implantation (1.5keV, $1E15cm^{-2}$) combined with Ge pre-amorphization and optimized FLA. The sheet resistivity was 770 Ω/sq. about 1/3 to 1/4 of that without Ge PAI. This enhanced activation for Ge PAI case is due the increase in energy absorption at the Si surface. The relationship between sheet resistivity and Xj shows much lower sheet resistivity and shallower pn junction can be realized FLA as compared with conventional spike RTA.

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