Single and few electron devices Integration trends

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Single Electron Transistors (SETs) are considered to be promising candidates for high density and very low power integrated circuits. One of the reason is their ability to be scaled down to nanometer size. These devices have also some specific features, such as Coulomb Blockade Oscillations (CBO), that MOSFET have not. However there are some constraints and physical limitations. In this presentation, we will review the different solutions which have been explored to fabricate and optimize SETs and we will give the trends. We will also discuss the potential application of these devices to integrated circuits, based on their operation and properties, in comparison with those of MOSFETs.

Fabrication

From the first Single Electron Transistor [1], many approaches have been explored to improve their characteristics and to increase their maximum operating temperature. Whereas sub-100mK is acceptable for physical experimentation, 300K is mandatory for circuit applications. The main difficulty is the size requirement, since nanometer dimensions are really needed to get a charging energy well above the thermal energy, while achieving a sufficient level of uniformity and reproducibility. Unfortunately, this is beyond the present resolution of conventional lithography equipments.

In a first group of approaches, the main target has been to reduce the size of the islands where electrons are confined. This has been done by evaporation or deposition of metallic clusters [2] or colloid materials in a gap between electrodes. With such solutions, non linear I(V) characteristics and Coulomb gaps are obtained but CBO are rarely observed. At LETI, we have developed LPCVD processes for the deposition of nanometer Si clusters. The impact of the substrate material and chemical treatment on the density of nucleation site have been investigated and a reproducible Si-QDs density higher than $10^{12}/cm^2$ has been achieved, which is the highest value reported for the CVD technique [3]. This is suitable for nano-crystals memories [4], but the tunnel gap between adjacent islands is not yet sufficiently controlled for application to lateral SETs. By AFM manipulation of particles these gaps can be individually tuned [5], nevertheless this is obviously not convenient for the fabrication of complex circuits.

Atomic Force Microscopy tools have also been used for the fabrication of SET and Multi Tunnel Junction (MTJ) structures by local oxidation under the tip of a thin layer of metal. In that case, the device geometry is well defined and the metal island can be very small, however, the tunneling barriers have a thickness of several nm which results in a very low level of current [6].

Another approach to obtain nano-islands with a size well below the lithography resolution is to take advantage of some effect occurring at that scale. An example is the natural formation of potential islands along a silicon nanowire as a result of fluctuations of the dopant concentration [7]. In the case of highly doped nanowire the formation of islands can also be attributed to a combination of structural roughness and segregation effects during thermal oxidation. As another example, in ultra thin polycrystalline-silicon film or wire the grain boundaries act as tunnel junctions and grains play the role of islands [8]. One again, a small size is obtained at the detriment of reproducibility.

On the opposite, by local depletion of a two-dimensional electron gas (2-DEG) with a set of electrodes, well defined quantum point contacts and dots have been fabricated. The size of the islands and the coupling strength can be varied. Artificial atoms and molecules have been studied on such structures, but single electron behavior is only obtained at low temperature due to the quite large size of the islands [9]. More promising, novel SETs with sidewall polysilicon depletion gates have been fabricated recently on silicon-on-insulator (SOI) nanowire. Reproducible Coulomb gaps and CBO periods are observed up to 77K [10].

Others techniques have been developed for the fabrication of silicon SET in which there is a self-aligned formation of both the island and the junctions on pre-patterned thin SOI layer. One is the PADOX process from NTT [11]. In another approach, a nanometer size quantum dot is formed in a silicon point contact, resulting in a large electron addition energy above 250meV [12]. For this structure, the mechanism underlying the formation of the dot and junction is not yet clear. In fact, whereas SETs are generally viewed and modeled as composed of a conductive island isolated by two dielectric tunneling barriers, there are some theoretical indications that resistances much higher that the quantum of resistance would be sufficient to confine electrons [13]. This is consistent with recent experimentations performed at LETI [14], opening new ways to fabricate SETs.

Circuits applications and discussion

Several silicon SET or hybrid MOSFET-SET logic gates, elementary functions and memory cells have been reported [11, 15]. They demonstrate that SETs are not any more laboratory objects but they have a real potential for circuits applications. The operation and properties of SETs and MOSFETs are different, but, since there is a process compatibility, it would be profitable to take advantage of the best of each [16]. Moreover, one can notice the common convergence towards SOI substrate. There are however some difficult challenges to overcome, especially the sensitivity of SETs to background charges. A better control of the material or background charges tolerant circuits are needed.

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References

[1] T. Fulton, G. Dolan, J. Phys. Rev. Lett. 59 p.109, 1987
[2] C. Vieu et al, J. Vac. Sci. Tech. B 16 (6), p3789, 1998
[3] F. Mazen et al, accepted for publication in JECS
[4] A. Fernandes et al, IEDM 01 Tech. Dig., p.155, 2001
[5] S. Carlsson et al, APL 75 (10), p.1461, 1999
[6] Y. Gotoh et al, JJAP 41 Part 1 N°4B, p.2578, 2002
[7] G. Evans et al, JJAP 40 Part 1 N°10, p.5837, 2001
[8] K. Yano et al, IEDM 93 Tech. Dig., p.2121, 1993
[9] R. Haug et al, Nanotechnology 7, p.381, 1996
[10] D. Kim et al, IEEE Trans. ED 49 N°4, p.627, 2002
[11] Y. Takahashi et al, ESSDERC Tech. Dig. p.61, 2002
[12] M. Saitoh et al, JJAP 40 Part 1 N°3B, p.2010, 2001
[13] V. Krupenin et al, JAP 90 N°5, p.2411, 2001
[14] D. Fraboulet et al, ESSDERC Tech. Dig. p.395, 2002
[15] H. Sunamura et al, Si Nano. Workshop, p.69, 2002
[16] A. Toriumi et al, Physica B 272, p.522, 1999