Achieving low junction capacitance on bulk Si MOSFET using SDOI process

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INTRODUCTION

The major advantage of SOI MOSFET over bulk Si MOSFET is the extremely low junction capacitance. However bulk Si MOSFET remains to be mainstream. This is mainly due to SOI's higher wafer cost and the difficulty in dealing with its floating body effect[1,2,3], In this paper we describe a new process, SDOI, to achieve extremely low junction capacitance on bulk Si MOSFET. SDOI stands for Source Drain On Insulator. It allows the source and drain region of a MOSFET to stay over an oxide layer while the channel region remains on bulk Si. The resulted junction capacitance reduction is similar to that of SOI. Unlike SOI MOSFET, SDOI MOSFET has no floating body effect, it does not require special device models and it can be easily integrated with other bulk Si devices, such as diodes and bipolar transistors.

PROCESS FLOW

The SDOI process flow is illustrated in Figure 1. Two masks are needed to define active area as shown in Fig. 1(b). The first mask defines the channel region which is bulk Si and the second mask defines the source and drain region, which is over oxide. The SDOI process starts with standard STI formation using mask No.1, followed by a photo step using mask No. 2, which opens up source, drain and channel region. The field oxide is then partially etched with high selectivity to nitride, as shown in Fig. 1(d). After resist strip and clean, 1000Å epitaxial Si is grown selectively from the side wall of the exposed Si region. 2000Å amorphous Si is then deposited over the epi-Si in Fig. 1(f). The amorphous Si and epi-Si are then polished back using CMP with high selectivity to oxide and nitride, Fig. 1(g). The nitride layer that covers the channel region is stripped in hot phosphorous. From this step onward the process follows the same bulk Si process.

RESULTS

The SDOI process has been developed on 0.13µm transistors. The selective epi-Si growth is key for SDOI MOSFET to maintain high channel mobility. Figure 2 shows the TEM cross section of an SDOI transistor. The DC characteristic of the SDOI MOSFET matches very closely to that of traditional bulk Si MOSFET. There is virtually no difference in sub threshold characteristic and drive current. SDOI source/drain junction leakage shows 30-50% reduction due to reduced junction area. SDOI shows 18% speed gain over bulk Si on fanout = 1 ring oscillator. The ring oscillators with heavy junction load show up to 30% speed gain. The SDOI MOSFET was found to have good tolerance to SDOI layer thickness variation. The process is highly manufacturable with the addition of a few design rules to avoid dishing during Si CMP.

CONCLUSION

We have manufactured SDOI MOSFET using bulk Si wafers to achieve junction capacitance as low as that of SOI. It improves switching speed by 18% compared to traditional bulk Si MOSFET. It could become a low cost alternative to SOI.

REFERENCES

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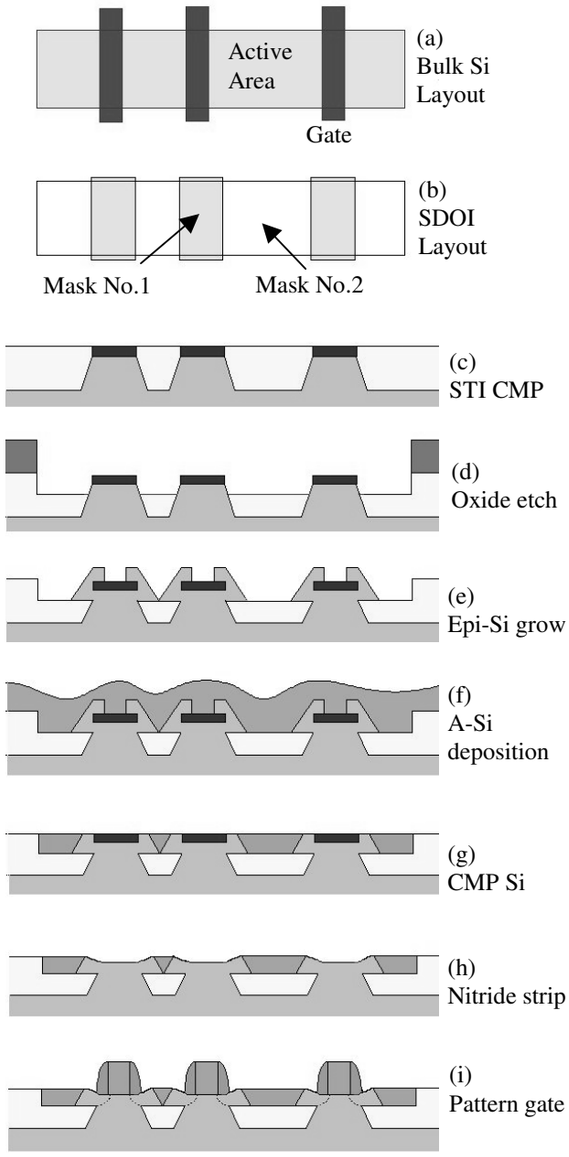

Figure 1. SDOI process flow

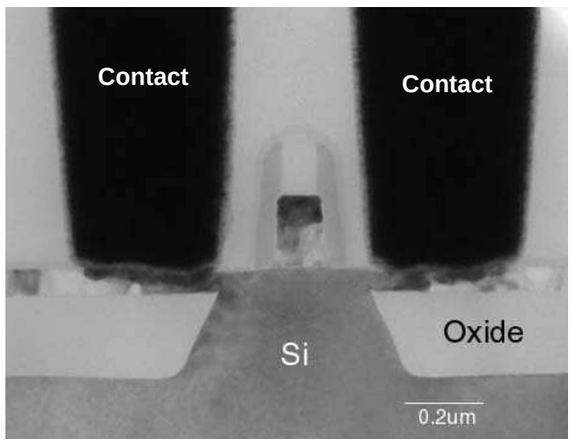

Figure 2. 0.13µm SDOI MOSFET cross section