Emerging Device Solutions for the post-classical CMOS era

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In pushing the scaling limits down to sub 50 nm devices it is well known that classical CMOS will reach its limits. Innovative processes, materials and/or device architectures will be required to overcome the major bottlenecks.
In this paper a short overview of the challenges of scaling will first be presented and the major bottlenecks will be identified. These are related to both physical and technological limitations. The most likely solutions as perceived in the recent international roadmaps will be discussed in more detail. These are:

- Fully depleted SOI devices
- High mobility CMOS based on Strained Si/SiGe layers
- Vertical devices
- Double and gate all around devices

Recent IMEC results on some of these new architectures will be presented as well. For each of the specific device architectures the specific process issues involved will be covered and electrical results that were obtained will be shown.
For Fully depleted SOI the process used is based on elevated source/drains using a spacer/replacer concept. This offers unique advantages with respect to process flexibility and performance [1].
For PMOS devices with strained SiGe in both single and multiple quantum well configurations, considerable mobility enhancements have been achieved. Process issues related to the presence of the SiGe layer have been solved adequately [2].
The vertical devices that have been realised are based on the presence of a heterojunction between source and channel: this prevents drain induced barrier lowering to deteriorate the device behaviour [3].
Finally for the multiple gate devices some achievements on double and triple FINFET-like structures will be given. A process will be presented which is directly CMOS compatible.
In conclusion indications for future work will be given.

References

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3. De Meyer, K.M.; Caymax, M.; Collaert, N.; Loo, R.; Verheyen, P.: *"The vertical heterojunction MOSFET"*. Thin Solid Films. Vol. 336: (1-2)299-305;1999.