Modeling End-of-the Roadmap Transistors

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The modelling of the end-of-the roadmap transistors and beyond faces issues associated with incorporation of new materials in the device structure, increasing role of quantum mechanical effect, extreme non-equilibrium transport and the discreteness of charge and matter, which introduces substantial intrinsic parameter fluctuations. Although conventional MOSFETs with 15 nm gate lengths have been demonstrated [1] they are likely to reach scaling limitations somewhere between 15 and 10 nm gate lengths due to saturation in performance and excessive gate and band to band tunnelling leakage [2]. The double gate architecture is a promising candidate for scaling MOSFETs to dimensions below 10 nm [2] according to the requirements of the Silicon Roadmap in 2016 and beyond. With improved gate tunnelling leakage current due to relaxed oxide thickness requirements and lack of channel doping it is believed that the scaling limitations of double gate devices will be determined mainly by direct source-to-drain tunnelling.

The sub 5 nm double gate MOSFET illustrated in Fig. 1 is a truly molecular scale devices. The randon dopant fluctuations in the source and drain regions, variation in the oxide thickness across the device, stray charges in the channel region, line edge roughness (LER), material composition and strain variations within the devices, all will introduce significant intrinsic parameter fluctuations. Due to the steady reduction in supply voltages and increasing count of transistors per chip such intrinsic parameter fluctuations will adversely affect the functionality and the yield of the next generations integrated circuits and are likely to become one of the major scaling limitation factors [4].

Here we present a methodology for statistical 3D 'atomistic' semiconductor device simulations which include quantum confinement and source-to-drain tunneling effects. The quantum corrections are introduces using the density gradient formalism and the simulator is carefully calibrated against comprehensive non-equilibrium Green's function simulations. We investigate (see Fig. 2) the impact of the source-to-drain tunneling on the operation of sub-10 nm double gate MOSFETs. As can be seen in Table 1 the tunneling affects adversely the subthreshold slope in these devices. We also study the intrinsic parameter fluctuations introduced by random discrete dopants, stray charges in the channel region and line edge roughness in sub-10 nm double gate MOSFETs. Fig. 3 illustrates the impact of the line edge roughness on the threshold voltage fluctuations in sub 10 nm devices. The statistical rough gate edges used in the simulation study are generated assuming a Gaussian autocorrelation function. RMS amplitudes much smaller than the best achievable today produce fluctuations commensurable with the expected supply voltages for this generation devices.

[1] B. Yu, H. Wang, A. Joshi, Q. Xiang, E. Ibok and M.-R. Lin, IEDM Tech. Dig., pp. 937-941, 2001
[2] H.-S. P. Wong, IBM Journal of Research and Development, Vol. 46, pp. 133-168, 2002
[3] International Technology Roadmap for Semiconductors, The 2001 edition
[4] H. P. Tuinhout, Proc. ESSDERC 2002, eds. G. Bacarani, E. Gnani, and M. Rudan, pp.95-101.

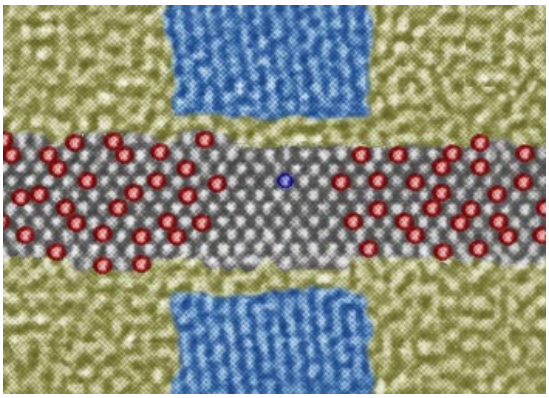

Figure 1: Impression of a 4 nm gate length double gate MOSFET illustrating some of the sources of intrinsic parameter fluctuations. The picture is designed using Photoshop™ and real TEM images of the Si/SiO_2 Poly-Si/SiO_2 interfaces.

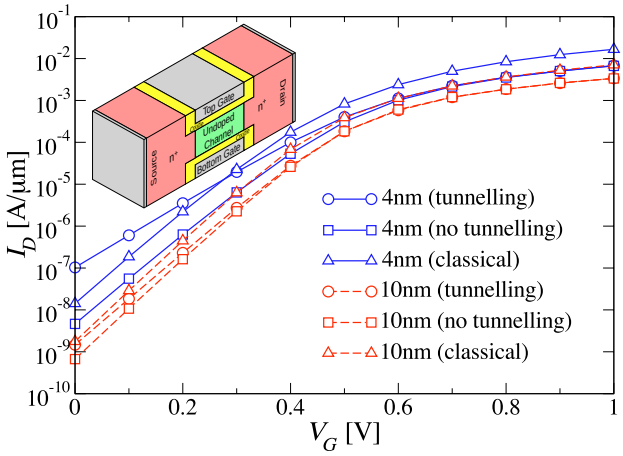

Figure 2: I_D-V_G characteristics for double gate MOSFETs with gate lengths of 4nm and 10nm obtained from density gradient with and without source-drain tunnelling, and from classical simulations. A schematic illustration of the simulated double-gate MOSFET is shown as an inset.

	Tunnelling	No Tunnelling	Classical
4 nm	132 mV/dec	96 mV/dec	94 mV/dec
10 nm	92 mV/dec	84 mV/dec	84 mV/dec

Table 1: Subthreshold slopes calculated for the I_D-V_G curves presented in Fig. 4.

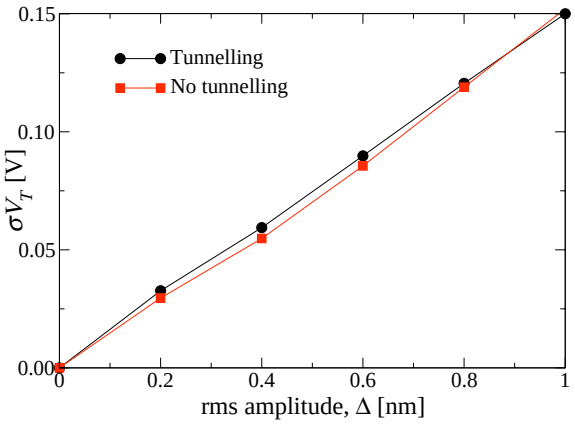

Figure 3: Standard deviation in threshold voltage, σV_T, due to LER with rms amplitude Δ for 4nm double gate MOSFETs. Correlation length Λ = 5nm.