Thin Film Transistors in ULSI –Status and Future

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The current status of the thin film transistor (TFT) in ULSI is reviewed. The problems and solutions are discussed. Possible future applications of TFTs to ULSI and related fields are examined. Nanosize TFTs are potential solutions for many current problems but create technical challenges for scientists and engineers.

In the conventional ULSI chip, all transistors are fabricated based on the single crystal characteristics of the silicon wafer. Only one layer of transistors can be fabricated on the substrate. The TFTs can be fabricated on a variety of substrates, such as the dielectric or even polymeric surface, as long as they can withstand the process conditions, such as temperature. The TFT structure is similar to that of the multilevel interconnect in ULSI, except the additional silicon and doping layers. In principle, the 3D circuit, as shown in Figure 1, can be fabricated by integrating TFTs with conventional ULSI transistors.

Due to the inferior material characteristics, the a-Si:H TFT, which has an interface density of states several orders of magnitude higher than that of the single crystal silicon, is improper for ULSI applications. The poly-Si TFT can have a field-effect mobility as high as 500 cm^2/Vs, which makes it possible for some logical applications. However, the poly-Si TFT technology involves complicated material, process, and device issues.

The poly-Si material contains a large number of defects at grain boundaries and, sometimes, within the grain. These defects can be reduced by methods such as hydrogenation or high temperature annealing. However, for ULSI applications, TFTs are fabricated above the silicon wafer where a large number of conventional transistors have been pre-fabricated. The process temperature needs to be low to prevent any damage to existing devices. Since it is well known that the hydrogenation process can damage the single crystal silicon, its influence to the ULSI silicon transistor needs to be investigated.

There are many low-temperature poly-Si TFT fabrication processes, such as laser, long-time thermal annealing, and metal-reduced crystallization. Most of them have practical limitations in the ULSI field. We will compare these methods and discuss individual issues with examples.

The poly-Si TFT has many unique device issues with regard to its mobility, I_{on}, I_{off}, threshold voltage, subthreshold slope, etc. Possible solutions will be reviewed and discussed. Most of them are based on new structures or fabrication methods. In addition, the reliability issue, which is critical in VULSI, will also be examined.

If TFTs can be fabricated into nanosize, the operation speed can be drastically increased. However, just like the conventional ULSI technology, many basic material problems need to be solved.

In addition to conventional 3D circuit applications, TFTs can be applied to many ULSI-related new areas, such as optoelectronic devices, e.g., TFT next to an optical device; TFT-driven optical, chemical, or physical sensors (on the top layers of the chip); phototransistors; TFTs on storage devices, e.g., on hard disks or CDs; TFT on biochips, etc.

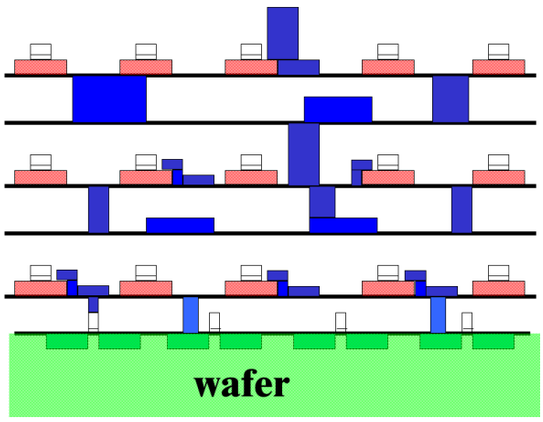

Figure 1 TFT Integrated 3D ULSIC