Extending The Life Of Planar Single-Gate CMOS & The Realization Of Double-Gate/Multi-Gate CMOS Devices

John O. Borland[1], Hiroshi Iwai[2], Witek Maszara[3] and Howard Wang[4]
1.VSEA, 4 Stanley Tucker Dr., Newburyport, MA 01950
2.-Tokyo Institute of Technology, Yokohama, 226, Japan
3.-AMD, One AMD Place, Sunnyvale, CA 94088
4.- TSMC, Hsinshu, Taiwan, 300, R.O.C.

The end of the roadmap for planar single-gate (SG) CMOS seems to be drawing nearer as the industry increases research activities in double-gate (DG) or multi-gate (MG) CMOS novel device structures. The 2001 ITRS roadmap classifies logic devices into three different categories: 1) high performance (HP) for desktop computers which are highly scaled, 2) low operating power (LOP) for portable mobile systems with limited battery life like notebook computers and 3) low standby power (LSTP) for cell phones requiring lowest leakage current [1]. Multiple device roadmaps are emerging depending on specific application (Fig.1) [2]. Different logic and memory applications will also require variations in transistor design from HALO to Super HALO, strain-Si channel for mobility improvement, source drain extensions (SDE) with elevated source drain (S/D) to lateral graded single S/D (LG-SS/D). Novel device structures will also vary from planar SG (P-SG) to vertical SG (V-SG) and eventually to DG and MG devices [3,4]. With the integration of these various transistor designs and novel device structures on the same chip for system-on-chip (SOC), new silicon wafer options are also emerging from traditional bulk Cz and Epi wafers to blanket SOI and new selective/patterned SOI wafers for partially depleted (PD/SOI) and fully depleted (FD/SOI) devices (Fig.2) [5-8]. Therefore, this paper will focus on extending the life of planar SG CMOS through 2016 and accelerating the understanding & realization of DG/MG CMOS by 2007 through the use of advanced ion implantation techniques. First a review of 300mm wafer technology will be given followed by advanced isolation technology. Then gate stack evolution followed by channel, source drain and contact engineering including shallow junction formation and the lateral graded-SDE (LG-SDE) and LG-SS/D structure (Fig.3) [7]. Finally, novel device structures including DG and MG CMOS devices will be discussed (Fig.4) [4,7].

References

1] ITRS-2001 PIDS roadmap (www.public,itrs.net).
2] H. Iwai, VSEA vTech seminar presentation material July 22, 2002 in San Francisco, CA.
3] Divakaruni and Bronner, the Electrochemical Society, PV2001-2, March 2001.
4] W. Maszara, MRS Symp. Proc. Vol. 686, p.59, 2001.
5] D. Sadana, VSEA vTech seminar presentation material July 22, 2002 in San Francisco, CA.
6] Yamada et al., VLSI Symposium 2002, section 12.1, June 2002.
7] J. Borland, VSEA vTech seminar presentation material July 22, 2002 in San Francisco, CA.
8] D. Volgar, WaferNEWS, p. 9, August 5, 2002.

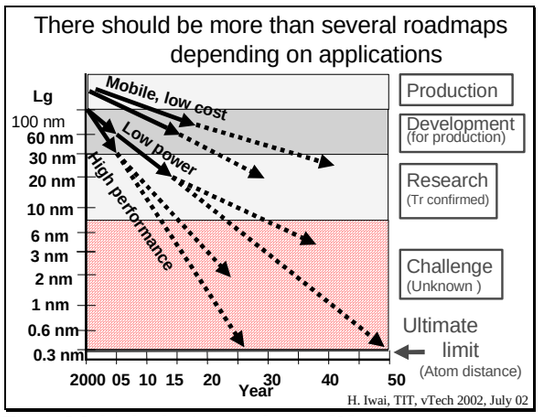

Fig.1: Multiple device roadmaps [2].

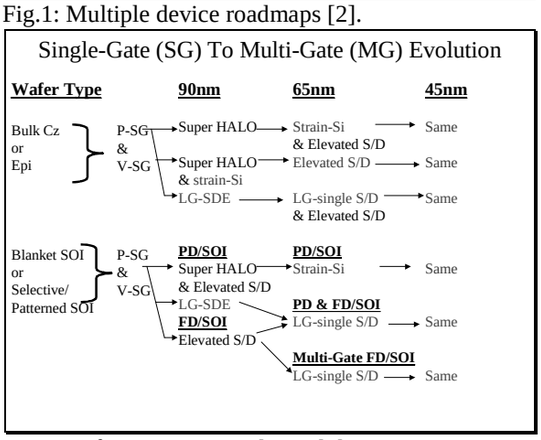

Fig2: Wafer, transistor and novel device structure evolution.

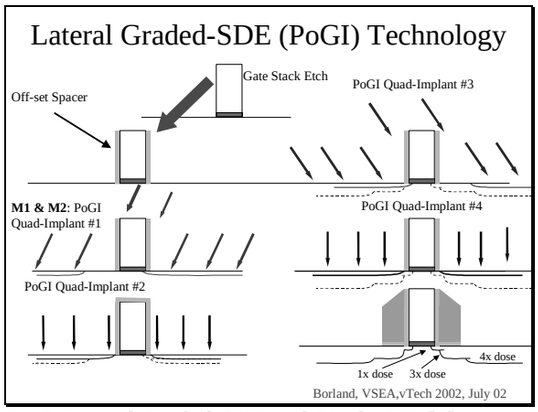

Fig.3: Lateral Graded-SDE and Single S/D [7].

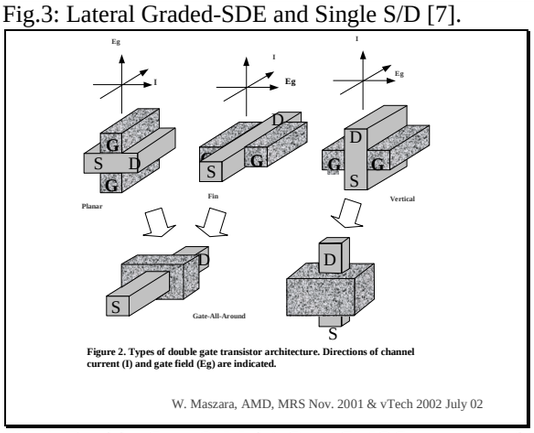

Fig.4: Double-Gate & Multi-Gate CMOS structures [4].