Si channel surface dependence of electrical characteristics in ultra-thin gate oxide CMOS

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Introduction

For high-speed logic applications, suppression of the power consumption is very important and thus supply voltage should be reduced at every new generation. In order to realize high performance despite a low supply voltage, gate oxide thickness has to be reduced continuously. In fact, it has been suggested that even 1.6 -1.1 nm EOT (equivalent physical SiO_2 thickness) gate insulator be used for 45 nm gate length MOSFETs in 100-nm technology node [1]. With thinning the gate oxides, the quality control of Si/insulator interface would dominate performance and reliability. It is also pointed out that high-k gate devices in future use would need interfacial layer between Si and high-k insulator in order to realize high quality of interface [2].

This paper reviews recent work concerning Si/ SiO_2 interface quality of MOSFETs, such as various Si surface channel orientations [3,4] and epitaxitial Si channel layer [5].

Si surface orientation

The properties of 1.5 nm gate oxides and the characteristics of the related CMOS transistors on (111) and (110) surface-oriented Si substrates were investigated and compared with those on (100) substrate. It was found that the behavior regarding low field mobility in n- and p-MOSFETs in 1.5 nm gate oxides is the same as in the thicker oxide case. Transconductance of p-MOSFETs on (110) substrate was 1.9 times greater than that for (100) substrates.

In thin oxide region, uniformity of oxide thickness and surface roughness, gate leakage current and 1/f noise are almost the same in (111) and (100) substrates. It was also found that reliability of (111) MOSFET is slightly better than that of (100) MOSFETs. Improved reliability in ultra-thin oxide MOSFETs on (111) substrate seems to be related with oxidation mechanism. TEM observation revealed the existence of a few one-layer steps at SiO_2/Si interface on (111) substrate. They support the model of layer by-layer oxidation reaction at the initial stage on (111) Si surface [6]. On the other hand, it was found that gate leakage current, 1/f noise and reliability of (110) MOSFETs are worse than those for (100) substrates due to larger interface roughness or inferior SiO_2 film quality.

Epitaxitial Si channel

The epitaxial Si channel technique is known to be effective for realizing high performance in small gate length MOSFETs. It was introduced for 1.5 nm gate oxide CMOS on (100) Si substrate. Improved drain current drive and transconductance of the epitaxial channel MOSFETs with ultra-thin gate oxide in the direct-tunneling regime were confirmed. It was found that the epitaxial Si channel noticeably reduces the direct-tunneling gate leakage current. The AFM and 1/f noise results suggest that the reason for the improved leakage current is the improvement of the oxide film quality such as roughness or defect density due to the crystal perfection and low contamination involvement of the epitaxial layer.

Conclusions

It was investigated how the interface quality affects electrical characteristics, such as mobility, direct-tunneling gate leakage current, 1/f noise characteristics and reliability in ultra-thin gate oxide MOSFETs. The improvement of the interface quality will be a key to the realization of ultra-thin EOT gate insulator CMOS in future generations.

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