Compatibility of PolySilicon with HfO$_2$-based Gate Dielectrics for CMOS Applications

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Hafnium-based materials such as oxides, silicates and aluminates of hafnium are being widely studied for application as high-K gate dielectrics to meet the needs of CMOS scaling. For rapid deployment of high-K gate dielectrics into existing CMOS lines, compatibility of the high-K dielectric with polysilicon gate electrodes is critical. It is therefore necessary to evaluate the stability of the high-K gate dielectric during polySi deposition and CMOS processing. Previous studies $[1,2]$ have reported that exposure to SiH$_4$ during CVD polySi deposition leads to reduction of HfO$_2$ and causes high leakage failures.

Capacitors were fabricated with HfO$_2$ films using polysilicon gate electrodes deposited by various CVD processes. Polysilicon was deposited using low pressure CVD or rapid thermal CVD under varying conditions as shown in Table 1 to obtain poly films that were either amorphous or crystalline as-deposited. The polySi was doped either by ion implantation of arsenic, or doping in situ during growth using phosphorus. Gate leakage current was monitored as a metric for compatibility and thermal stability. Dopant activation anneals were done at 700 and 1000°C.

A summary of the results is shown in Figure 1 showing leakage current versus poly recipe. Equivalent oxide thickness for the samples is ~1.9-2.4nm as indicated by the bars. The leakage current measured at 1V beyond flatband is seen to vary strongly with the poly deposition process. For the uncapped HfO$_2$ films, low temperature amorphous depositions show good leakage (A,B), while with crystalline polySi depositions (G,H) show lower leakage than the amorphous depositions. This is a useful result because for CMOS applications, it is likely that crystalline poly depositions are more favorable for meeting the criteria for gate depletion, boron penetration and Vth matching $[3]$.

Since CMOS applications will also typically require higher activation temperatures than 700°C, some of the samples were also annealed at 1000°C, the results of which are shown in Figure 2. Several of the crystalline recipes survive the 1000°C activation anneal but only when a capping layer is used. The high leakage observed for HfO$_2$ with crystalline furnace polysilicon electrodes is speculated as being due to the presence of weak spots or defects in the film which in the presence of a reducing ambient during polySi deposition such as silane (SiH$_4$), become high-leakage conduction paths. A possible mechanism of a conduction path is the presence of Si along the weak spots $[4]$ forming a conduction path. TOF-SIMS spectra suggest that there may be Si present within the HfO$_2$ film.

References: