Process Strategy for Built-in Reliability of Cu Damascene Interconnect System for 0.13um-Node and Beyond

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As the shrinkage of future sizes and the introduction of low-k material, the reliability issues in Cu metallization have become more serious. There are three reliability issues: EM (Electro-migration), SM(Stress-migration) and TDDB (Time-dependent dielectric breakdown), and it is important to solve these issues at the same time. In this report, we describe the process design strategy to achieve built-in reliability of these three issues for leading edge Cu damascene interconnect system.

EM(Electro-migration) is the most fundamental reliability issue in metallization. Fig.1 shows electro-migration test results of 0.18um via for two different direction of electron flow. IMBS(Ionized-Metal-Bias-Sputtering) which has superior bottom coverage obviously improves EM property when electron flows from M1 to M2[1]. This result reveals that the current crowding at the bottom corner of via, where barrier thickness is thinnest, strongly degrades via-EM property. On the other hand, IMBS and LTS-2 has the same distribution in case of electron flow from M2 to M1. C.K. Hu et al[2] reported that EM property in Cu damascene structure is dominated by the diffusion at the grain boundary and interface/surface and above mentioned result supports that the M1-Cu/capping dielectric interface affects the EM lifetime for electron flow of M2 to M1. From these results, we conclude that the preferential deposition at the bottom corner of via for the dispersion of current is the key to improve the via-EM property as well as the adhesion improvement at Cu/dielectric interface for suppression of Cu diffusion.

SM is the pressing issue which appears frequently as the pattern size is shrunk. There are two modes in SM problem. One is the stress induced voiding inside via, which is accelerated by high temperature baking in case of via having above wide Cu wire as is shown in Fig.2(b)[3]. The other is the stress induced voiding below via which is observed in wide Cu wire underneath via with low temperature aging such as 150-250^{o}C[4]. We investigated the several factors for these two mode SM issues and found the countermeasures to suppress these modes, which details will be described at the symposium[5].

TDDB is the additional issue in Cu metallization because the conventional Al,W metallization didn't meet this problem[6][7]. TDDB characteristics between 2 adjacent Cu wires are mainly dominated by the 2 factors. One is the intrinsic property of barrier material and low-k material[8]. The other is the surface conditions on Cu/ dielectric caused by CMP process[7][9]. Fig.3 shows the effects of NH3 plasma treatment just before SiN barrier deposition and the wet cleaning after Cu-CMP on TDDB lifetime. It is necessary to control not only metal barrier property and low-k property but also the surface condition of Cu-CMP surface.

The outline of process design for built-in reliability is summarized in Table.1. It is necessary to design the consistent process parameters for all reliability issues.

References
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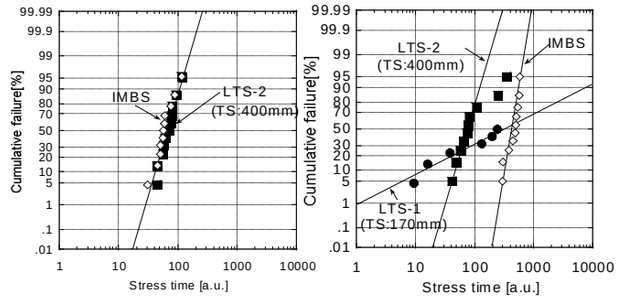
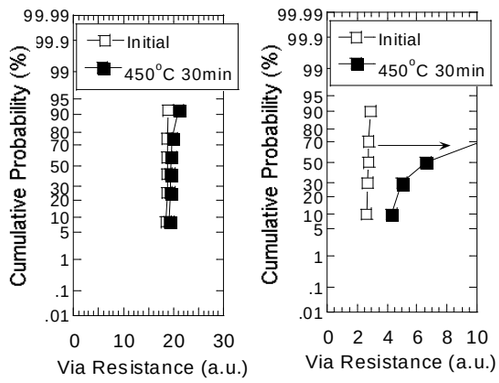


(a) e:M2 ->M1 (b) e:M1 ->M2

Fig.1 EM results of Cu wiring with 0.18um via.



(a)0.25 um wide Cu (b) 4.0um wide Cu

Fig.2 Distribution change of the via-chain resistance By annealing at 450^{o}C for 30 min.

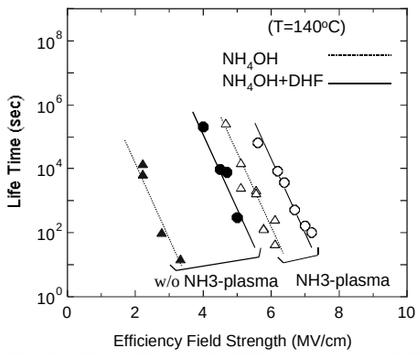


Fig.3 The effects of NH3-plasma and DHF cleaning on TDDB property.

Table.1 Outline of process design for built-in reliability in Cu metallization.

Items	Objects	Process parameters
EM	Cu Cu/barrier-ILD interface Barrier metal	Grain control Adhesion Preferential deposition at the bottom corner of via
SM	Cu low-k material Barrier Via bottom	Grain/stress control Adhesion to Cu Adhesion to Cu Residue free/shape control
TDDB	low-k material Barrier metal CMP surface	Cu diffusion Barrier property Cu oxide free/damage free