Impact of Wafer Backside Cu Contamination to 0.18 um node Devices

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In comparison to aluminum (Al), copper (Cu) interconnect technology provides better RC performance and higher electromigration reliability. For advanced semiconductor manufacturing (0.13 um and below), Cu interconnect has been implemented in many fabs. Due to the high cost of manufacturing equipment, many fabs want to share Cu process tools with Al technologies, but there exists a high risk and damaging impact of Cu contamination to semiconductor manufacturing. Cu is a fast diffusant in silicon [1], able to create deep level defects and also degrade the gate oxide integrity. Cu-contaminated ultrathin oxide exhibits enhanced oxide leakage currents, lower oxide breakdown voltage, and lower charge to breakdown (QBD) than uncontaminated wafers [2]. If Cu reaches transistors, it could cause detrimental impact to the devices. To prevent Cu diffusion to active devices from the front side, a silicon nitride film is usually used to separate the front end of line (FEOL) transistors from the back end of line (BEOL) Cu interconnect process. On the wafer backside, there may not exist a SiN film. For many shared tools, the back surfaces of Cu-processed wafers may be contaminated with Cu, and the contaminants may transfer to the backside of none Cu wafers. Therefore, it is critical to evaluate the impact of the Cu contamination at the wafer backside surface to the front side devices.

In this paper, we studied the effect of backside Cu on 0.18 um technology node wafers with Al interconnect. After the product wafers finished the Al BEOL process, half of the available dies (in a checker board pattern) per wafer were pre tested. The characterization includes transistor parameters and gate oxide integrity test for both thin and thick oxide. After the Al BEOL process, the wafer backside consists of at least the following films: oxide, polysilicon, and silicon nitride. To separate any possible Cu diffusion barrier impact for each film, we stripped SiN film to poly silicon in a hot HF solution. For some wafers, the poly and remaining oxide were further stripped to bare silicon in a HNO3:HF solution. About 50 A PVD copper film was deposited on wafer backside and then driven into Si at approximately 350C for 90sec. The backside Si received targeted removal to specific amount so that the backside Cu level ranged from none, 1E11 to 1E16 atoms/cm^2 as measured by TXRF. These wafers were annealed in N_2:H_2 for 7 hours in a furnace at temperatures ranging from 350 to 450C. All wafers were then electrically tested on the other half of the dies.

After backside Cu contamination and thermal anneal, the wafers do not show significant change in junction leakage current. Higher thermal annealing temperature shifts the threshold voltage (Vt) up to 17 mV. However, the increase of backside Cu contamination level and the removal backside film stack do not affect the Vt, as shown in Tables 1 and 2. No significant change in QBD of the thick and thin gate oxide area capacitors was observed for the wafers, even with 1.0E16 atoms/cm^2 of Cu and at a 450C anneal temperature. This is shown in Figure 1. Interfacial state density measured by charge pumping test shows a slight reduction for PMOS devices (as shown in Figure 2) after Cu contamination and anneal. This may be primarily due to the impact of thermal anneal. All these results suggest that backside Cu may not significantly affect 0.18 um node devices during standard BEOL thermal process with bare Si, poly or SiN film on the backside. In addition, we will also report the Cu diffusion from wafer backside by SIMS and ESCA analysis.

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1. DL Kendall and DB DeVries, Semiconductor Silicon (New York: Electrochemical Society), pp. 358 (1969)
2. Y.H. Lin et al, J. Electrochem. Soc. **148**, F73 (2001)

Cu Concentration (atom/cm^3)	Anneal Temperature		
	450C	400C	350C
1.0E+16	15.3 mV	14.3 mV	5.3 mV
1.0E13 - 1.0E14	16.3 mV	11 mV	7.1 mV
1.0E12 - 1.0E13	16.8 mV	13.6 mV	8.3 mV
1.0E11 - 1.0E12	17 mV	11.5 mV	9.1 mV
< 1.0E11	10.8 mV	10.6 mV	8.9 mV
None			8.3 mV

Table 1: VTP shift vs. Cu contamination levels for bare Si backside wafers.

Backside Film	Temperature/Cu Conc		
	450C		400C
	1.E+16	None	None
SiO2+ Poly +SiN	13.1 mV	11.3 mV	12.5 mV
SiO2+ Poly	12.3 mV		

Table 2: VTP shift vs backside film stack post Cu contamination.

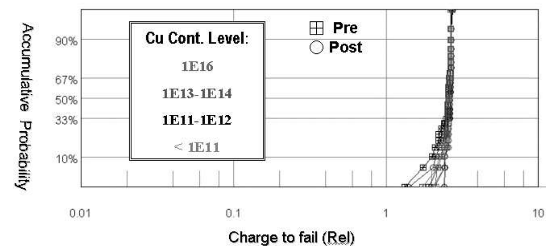

Figure 1. QBD of area capacity pre and post Cu contamination and anneal at 450C.

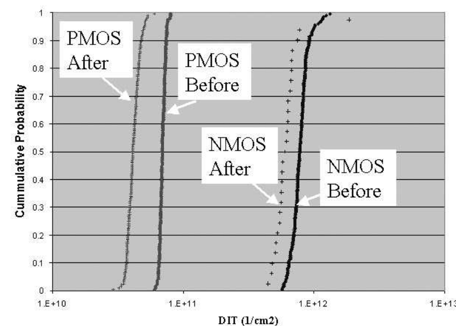

Figure 2. Interface state density pre and post backside Cu contamination and anneal.