Electrical Characteristics and Thermal Stability of $W_2N/Ta_2O_5/Si$ MOS Capacitors in Nitrogen or Hydrogen Ambient

P. C. Jiang and J. S. Chen
Department of Materials Science and Engineering
National Cheng Kung University
Tainan, Taiwan

The poly-Si/SiO_2 stack has been used as the MOS (metal-oxide-semiconductor) gate structure for decades. As the gate oxide thickness decreases to below 2 nm for sub-100nm generation, gate leakage currents will be amplified due to the direct tunneling effect. To overcome this problem, high dielectric constant materials are employed because they may exhibit low leakage currents due to thick physical thickness. In addition, metal nitride gate electrodes have been proposed because metal nitrides have low resistivity and will not show gate depletion. Therefore, the metal nitride/high-k oxide stack will be an interesting structure for gate application.

In this study, W_2N and Ta_2O_5 are chosen as the gate electrode and the gate dielectric, respectively. The thermal stability and electrical properties of $W_2N/Ta_2O_5/Si$ MOS capacitors were investigated after annealing at 400-600℃, in N_2 or H_2 ambient.

N-type (100) silicon wafer was cleaned by a modified RCA clean and then dipped in 1% HF solution for 1 min. After cleaning, the Ta_2O_5 film was deposited on the Si substrate by MOCVD. The total chamber pressure was controlled at 1 Torr and temperature was set at 450℃. After deposition, the Ta_2O_5 film was annealed in oxygen at 800℃. W_2N gate electrode was then deposited on annealed Ta_2O_5 layer by reactive sputtering. After the MOS structure was completed, samples were annealed at 400-600℃ in N_2 ambient or at 400-500℃ in H_2 ambient for 30 min, to investigate their thermal stability.

Fig. 1 shows the GIAXRD spectra of $W_2N/Ta_2O_5/Si$ samples after annealing at 500℃, in N_2 or H_2 atmosphere. WO_3 phase appeared in the N_2 annealed sample, but not in the H_2 annealed sample. The W_2N gate is thus partially oxidized after annealing at 500℃ in N_2. Formation of WO_3 should be attributed to the residual oxygen gas in the annealing furnace.

High frequency C-V curves of the as-deposited and annealed MOS capacitors are shown in Fig. 2. After annealing, the C-V curves shift to the left. The C-V shift of the H_2 annealed sample is less than that of the N_2 annealed sample. The result indicates that annealing in N_2 ambient will more significantly increase positive charges, or reduce negative charges in the oxide layer than annealing in H_2 ambient.

Fig. 3 shows the I-V characteristics of the various MOS capacitors. The leakage current decreased after annealing in N_2 ambient at 600℃. It should be attributed to the oxidation of W_2N gate electrode. MOS capacitors annealed at either 400℃ or 500℃ in H_2 ambient show I-V curves similar to that of as-deposited one. However, the leakage current increases with increasing annealing temperature when annealing in N_2 ambient, at 400-500℃.

In conclusion, after annealing $W_2N/Ta_2O_5/Si$ MOS capacitors in N_2 at 500℃, the W_2N gate would partially oxidized to WO_3. Annealing MOS capacitors in both H_2 and N_2 ambient will slightly increase the leakage current, and induce the change of charges in the oxide layer. However, the $W_2N/Ta_2O_5/Si$ MOS structure shows a superior thermal stability when annealing in H_2 ambient than in N_2 ambient.

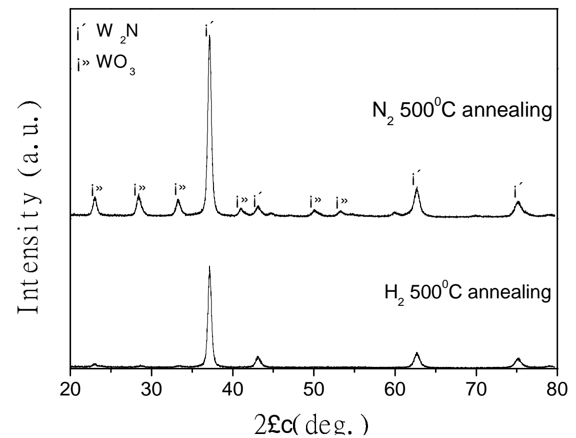

Fig. 1 GIAXRD spectra of $W_2N/Ta_2O_5/Si$ samples after annealing at 500℃ in N_2 or H_2.

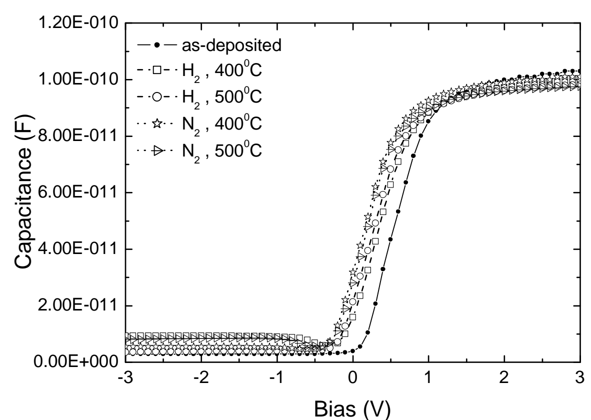

Fig. 2 High frequency C-V curves of as-deposited and annealed MOS capacitors.

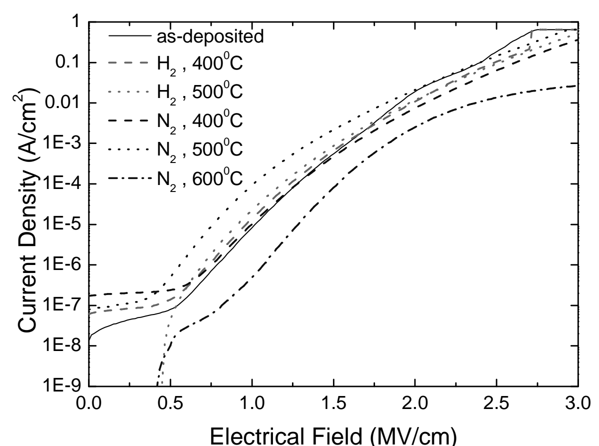

Fig. 3 I-V curves of as-deposited and annealed MOS capacitors.