STUDY OF SUB-QUARTER-MICRON PMOSFET NBTI UNDER DC AND AC STRESS

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The threshold voltage (V_T) shift in PMOSFETs due to NBTI (Negative Bias Temperature Instability) has been investigated long time ago [1,2]. Recently, It is reported that PMOSFET V_T shift becomes worse in the nitrided gate dielectric than in thermal oxide [3]. This has become a major reliability concern for analog and mixed signal design.

While significant attention has been paid to DC NBTI effect, not enough study exists relating it to device degradation in real circuits. In this paper, the V_T shift of PMOSFETs under DC stress condition depended upon channel length, channel width, and temperature is studied in detail. The V_T shift under the worst case DC operating condition is also extracted from the experimental data. The impact of gate pulse frequency and duty cycle on PMOSFET V_T shift under AC stress condition is studied.

At elevated temperature, both 22 Å and 64 Å PMOSFET V_T shift can be observed even at the worst case operating voltages. To monitor the impact of interface trap generated during NBTI test, charge pumping current was also monitored at room temperature [4]. The charge pumping current measurement shows that interface traps are also generated during the stress [1]. The generated interface traps can only account for 7% of thin oxide device V_T shift and 20% of thick oxide device V_T shift, consistent with the degradation mechanism proposed.

Temperature has significant impact on NBTI effect. The extracted activation energies for thin and thick oxide devices are shown in Fig. 1. It is 0.38 eV for 22 Å 10/0.13μm PMOSFETs and 0.31 eV for 64 Å 10/0.24μm PMOSFETs, close to the values reported.

To study the degradation due to NBTI under AC stress, the "detrapping effect" has to be investigated first. In our study, the stress voltage is –1.8 V for 22 Å PMOSFETs and it is –4.5 V for 64 Å PMOSFETs. The devices were stressed for 100 minutes and, then, the stress voltage is changed to zero for 100 minutes to monitor the detrapping effect. This sequence goes on.

During the detrapping phase, the healing effect is significant. More than 80% of damage is recovered at room temperature. Thin oxide devices recover more than thick oxide devices. The following stress has smaller degradation slope compared with the first stress, as shown in Fig. 2 (a) and (b). At elevated temperature, the "detrapping effect" becomes less effective and only 50% of the damage is recovered, but the recovery time is smaller at elevated temperature.

At detrapping phase, the charge pumping current decreases insignificantly; positive charge trapping is the dominant degradation mechanism for NBTI stress. In thick oxide devices, the generated interface traps have significant impact on V_T shift at the end of detrapping phase.

The PMOSFETAC V_T lifetime are shown in Fig. 3. The V_T lifetime becomes larger as the pulse signal frequency increases.

[1] C. E. Blat et al, J. Appl. Phys., 1991, pp. 1712-1720.
[2] B. Doyle et al, *IEDM Tech. Dig*., 1991, pp.529-532.
[3] Chuan H. Liu et al, IEDM, Dig., 2001. pp 861-864.
[4] G. Groeseneken et al, *IEEE-ED*, 1984, pp. 42-53.

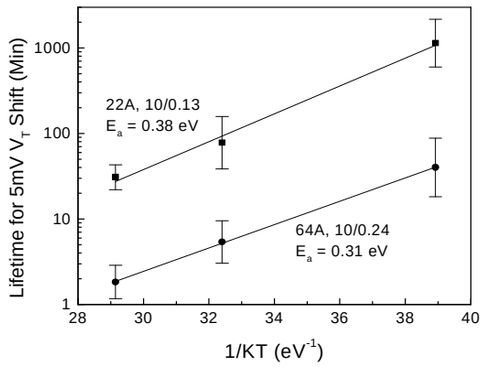

Fig 1. The dependence of PMOSFET lifetime on stress temperature. Vstrss is –1.32 V for 22 Å PMOSFETs and -3.63 V for 64 Å PMOSFETs.

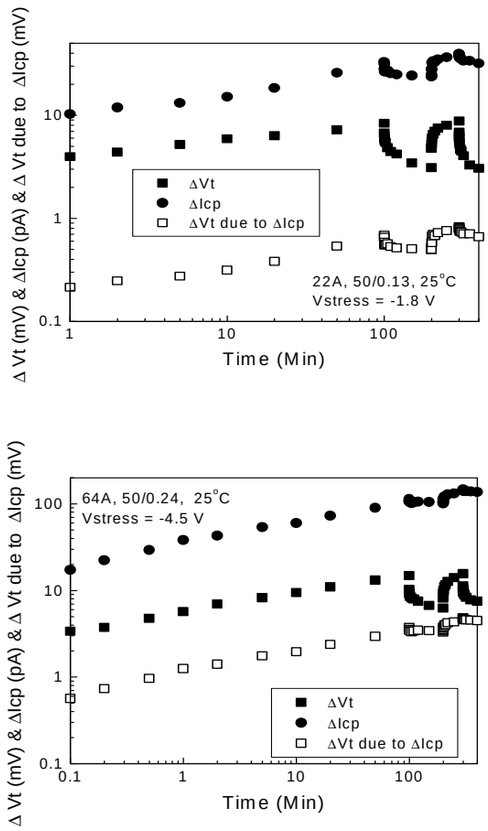

Fig. 2. Threshold voltage recovery and the change of charge pumping current during stress. (a) 22 Å PMOSFET (b) 64 Å PMOSFET.

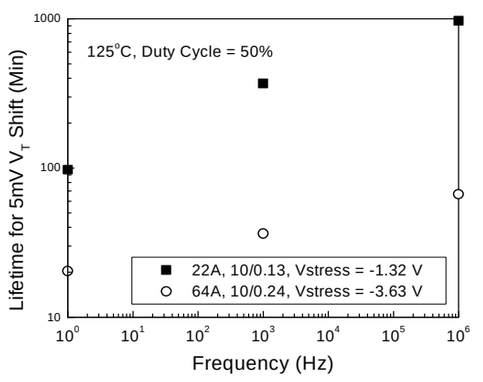

Fig. 3. PMOSFET AC NBTI vs. frequency at 125°C.