Fabrication of Sub-micron Active Layer SSOI Substrates using Ion Splitting and Wafer Bonding Technologies

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Mm-wave reflect-array simulations indicate a requirement for high frequency diodes with minimised 'on' resistance, thus requiring substrates with tight control of the thickness of the active silicon region beneath the device junction, combined with low resistance buried layer interconnects. As a realistic low-cost alternative to MBE-produced structures, this paper reports the fabrication of SSOI (Silicon on Silicide On Insulator) substrates with active silicon regions only 0.5μm thick, utilising low resistivity tungsten silicide (WSi_x) as the buried layer interconnect, produced using ion splitting and wafer bonding technologies.

Production of 0.5μm active layer SSOI substrates by wafer bonding presents a challenge in that the standard grind and polish back technique is suitable only for micron-plus SSOI, unless a complex polish-stop process is employed [1]. Direct ion splitting by implanting through the WSi_x layer results in thickness non-uniformities in the resultant SSOI active layer. Therefore a novel double-bond SSOI process utilising an intermediate ion split SOI bonded substrate has been developed. Ion splitting was performed by implanting hydrogen into the active wafer, bonding it to an oxidised handle wafer, and annealing at 500°C, causing the active wafer to split at a depth corresponding to the projected range of the hydrogen implant, and transferring a 0.5μm silicon layer to the oxidised handle wafer. Finally the SOI wafer was annealed at 1050°C to strengthen the interface bond.

Onto this SOI structure was deposited 0.35μm WSi_x and 0.8μm polysilicon, which was then polished to give a bondable surface. Separate high resistivity silicon (HRS) handle wafers ($\rho > 10k\Omega$-cm) have been processed with 1μm thermal oxide, which have been bonded to the ion split SOI / WSi_x / polysilicon wafers. The sacrificial silicon and silicon dioxide layers are then removed by grinding and selective chemical etching, resulting in the required SSOI structure. This process sequence is shown schematically in Figure 1.

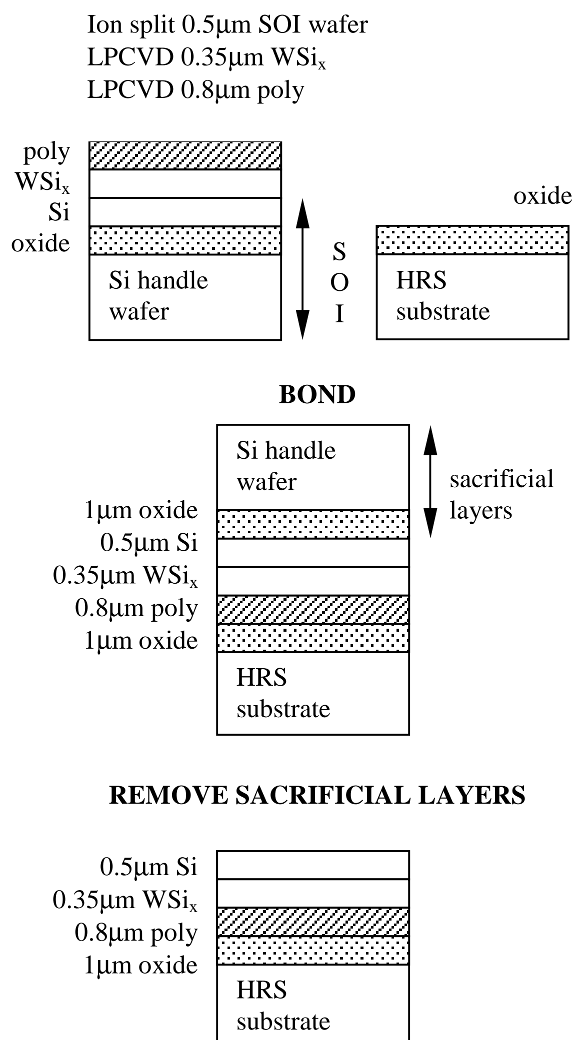

Fig. 1. Schematic process sequence for fabrication of sub-micron SSOI substrates

The bond interface between the ion split SOI wafer and the oxidised silicon handle wafer has been examined using an infrared microscope and a scanning acoustic microscope (SAM). SAM analysis of a typical double-bond structure is shown in Figure 2, indicating that the bond interface is essentially void-free. The SAM has detected the expected void region around the rim of the wafer which corresponds to the hydrogen implant scan used in the ion split SOI process. The paper will include further structural analysis of the SSOI substrate, along with a discussion of high frequency diode applications.

Fig. 2. Scanning Acoustic Microscope image of double bonded SSOI wafer structure

[1] Baine PT et al, J. Electrochem. Soc., Vol.145, No.5, pp 1738-1743, May 1998