Breakdown Characteristics of a High-Voltage Lateral PMOS with LOCOS Gate on SOI

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High-voltage lateral devices formed on a thick bonded SOI wafer have become popular for fabricating display driver ICs [1,2]. A high-voltage lateral p-channel MOSFET (PMOS) with gate oxide thickness sufficient to withstand the high gate voltage over 100V is essential in building up a high-voltage output circuit in the display driver ICs. We have investigated the breakdown characteristics of the high-voltage lateral PMOS with thick gate oxide formed by LOCOS process on SOI (H_PMOS). This paper shows the results in comparison with those of the high-voltage lateral PMOS with typical gate oxide (L_PMOS) driven by logic voltage of 5V.

Figure 1 and 2 show the device structure and process flow of fabricated high-voltage lateral PMOSs, respectively. A 6-inch bonded SOI wafer with an active layer thickness of 10μm and a 1μm-thick buried oxide film was used. The gate oxide thicknesses of the H_PMOS and L_PMOS were 400nm and 20nm, respectively. The gate oxide layer of the L_PMOS was formed by thermal oxidation. A basic difference in the structure between both devices is the diffusion profile of the p-source layer. The p-source layer of the L_PMOS can be formed by self-alignment to the gate polysilicon, while that of the H_PMOS must be carried out before LOCOS process, as shown in Fig. 2. This results in the deeper p-source layer of the H_PMOS than that of the L_PMOS. From process simulations, the difference of diffusion depth between the n-well and p-source layers, that is indicated as "d" in Fig. 1, of the H_PMOS was estimated at about 2μm.

Figure 3 shows experimental results of the breakdown voltages of the fabricated devices as a parameter of the n-well dose. The breakdown voltage of the H_PMOS strongly depends on the n-well dose, while the L_PMOS has a constant breakdown voltage of -270V.

From device simulations, it is found that the potential distribution concentrates at the source-gate side when the high drain voltage is applied to the PMOS on SOI. This is due to the substrate bias effect [3]. Judging from this fact and the diffusion profiles of the p-source and n-well layers, the punchthrough between the p-offset and p-source layers occurs in the H_PMOS.

Figure 4 shows the breakdown voltage dependence on the p-offset length (lp shown in Fig. 1) in the H_PMOS. The n-well dose was varied. The device with the n-well dose of $2x10^{12}cm^{-2}$ has a constant breakdown voltage of -100V. This breakdown is limited by the punchthrough. On the other hand, the breakdown voltage of the device with the n-well dose of $7.5 \times 10^{12}cm^{-2}$ increases linearly with lp, and then becomes saturated at -220V beyond lp of 12μm. The breakdown voltage of -220V is due to the punchthrough between the p-offset and p-source layers. Below lp of 12μm the breakdown voltage is dominated by the junction between p-offset and n-drift layers.

From experimental results it is found that the blocking capability of the H_PMOS with LOCOS gate on SOI is susceptible to the ion implantation dose for the n-well layer, resulting that the punchthrough mode easily occurs in this device. So, more precise formation of the p-source and n-well layers are essential for the high-voltage lateral PMOS with LOCOS gate than the PMOS with typical gate.

References

[1] H. Sumida et al., In Proc. ISPSD'98, (1998) p. 137.
[2] K. Kobayashi et al., In Proc. ISPSD'98, (1998) p. 141.
[3] H. Sumida et al., Solid-State Electronics 41 (1997) 1773.

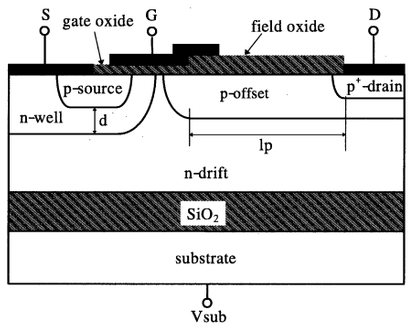

Fig. 1 Cross section of the fabricated high-voltage lateral PMOS on SOI.

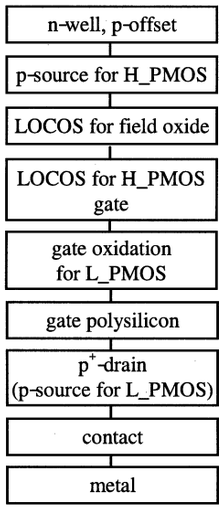

Fig. 2 Process flow for the fabrication of the PMOS.

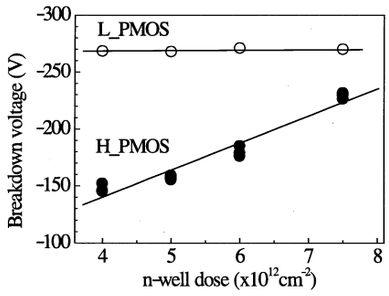

Fig. 3 Breakdown voltage dependence on the n-well dose.

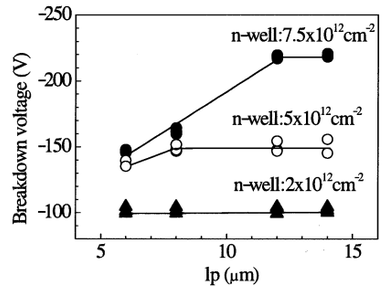

Fig. 4 Breakdown voltage dependence on lp in the H_PMOS.