Manufacture processes for GPSOI substrates and their influence on cross-talk suppression

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The performance of RF analogue circuits in integrated mixed signal telecommunications ICs can be compromised by cross-talk through the substrate from adjacent digital circuits. This problem becomes more severe as the frequency is increased, particularly for silicon-on-insulator substrates where the buried oxide becomes transparent to high frequency a.c. and transient signals [1]. The authors have previously demonstrated world-leading results on cross-talk suppression by using a GPSOI substrate, without the silicon active substrate, incorporating a buried WSi metallic ground plane [2]. The GPSOI was assessed using a standard reference coplanar waveguide test structure [1]. This uses both a transmitter pad and a receiver pad separated by distance d in a ground-signal-ground configuration. This paper addresses the structure shown in Figure 1, which includes the active silicon layer. The test structure has been modified to employ ion implanted transmitter and receiver diodes manufactured in the active layer. The GPSOI substrates have several variations. In some the ground plane was an n^+ implanted layer, while in others a WSi2 layer was employed. An additional trench feature was introduced on some structures and lined with silicide to form a Faraday Cage. This trench feature was either grounded by a top contact or the process was optimised to allow direct contact from the trench liner to the buried silicide ground plane. All substrates were manufactured using specialist bonding technology. This technology which employs polysilicon to bond the buried silicide layer will be described in detail. An SEM photograph of a typical structure is shown in Figure 2. The cross-talk measurements are shown in Figure 3. Reference SOI structures on both low and high resistivity handle wafers are included. The GPSOI substrate with WSi_2 ground plane shows a 30-40 dB reduction in cross-talk. This should be compared with a 15 –20 dB value obtained for diffused ground planes. The inclusion of the Faraday cage structure reduces the cross-talk by a further 30 dB to a value comparable to that achieved when no active layer is present. These represent the lowest cross-talk figures reported and verify a technology for cross-talk suppression.

Mixed signal substrates will include inductors. Ground plane technology is unsuitable for inductors as losses are increased due to image currents flowing in the ground plane. It is therefore essential to remove the ground plane from the inductor area prior to wafer bonding. In order to achieve planarity and high yield bonding, it is necessary to pattern the ground plane prior to bonding. The patterning of the WSi layer is achieved by selective dry etching of the silicide layer. After etching, a polysilicon layer is deposited over the WSi layer, filling the trenches created in the silicide. In order to produce a surface suitable for bonding, the polysilicon is planarised using standard CMP technology. The GPSOI substrate, incorporating patterned ground planes, is completed by thinning of the active silicon layer to the desired SOI thickness. This is achieved with conventional grinding and polishing techniques. The technology to produce this modified ground plane structure will be described in detail. In order to verify the effect the patterning of the ground plane has on the inductor, a simple test substrate was employed. The test substrate consisted of a WSi layer deposited onto silicon and patterned into pillars. An LPCVD silicon dioxide layer 1.8µm thick covers the silicide layer. Planar spiral inductors were fabricated on top of the test substrate. Substrates manufactured in this way show no degradation of the inductor quality factor. Relevant results for the inductor properties will be presented.

[1] J. Raskin et al, *IEEE Transactions on Electron Devices*, vol. 44, pp. 2252-2261, December 1997.
[2] J.S. Hamel et al, *IEEE Microwave and Guided Waves Letters* April 2000.

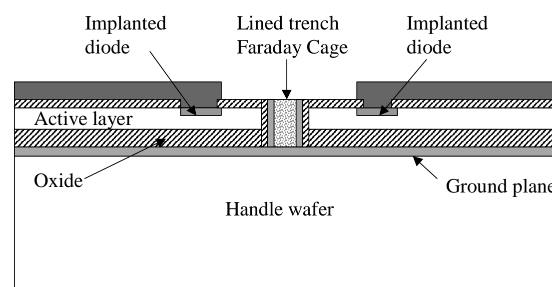

Fig. 1 Cross-talk test structure with implanted diodes in the active layer.

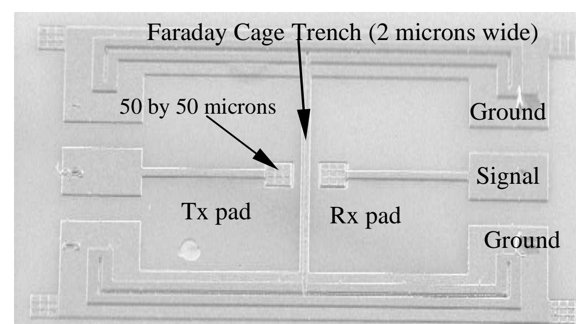

Fig. 2 SEM photograph (plan view) of the cross-talk test structure.

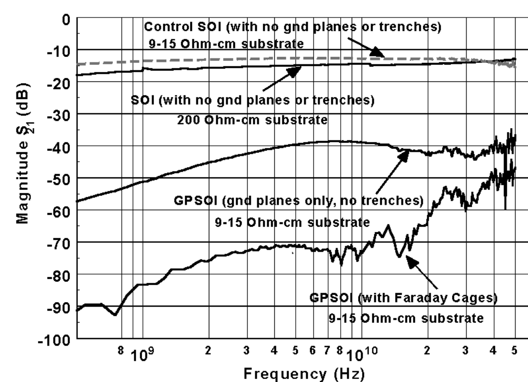

Fig.3 Measurement of transmission parameter for SOI and GPSOI structures.