Anodic Bonding and the Integration with Electronics

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INTRODUCTION

Anodic bonding is a method for joining glass to silicon, first presented by Wallis and Pomerantz [1]. It has been used in numerous microsystems in fields ranging from inertial sensors to optical and fluidic systems [2]. Due to the process' versatility, anodic bonding is also an attractive technology for packaging of monolithically integrated MEMS, where the micromachined structure and the read-out electronics are situated on the same silicon chip. However, high electric fields, elevated temperatures, and sodium contamination potentially deteriorate the electrical properties of anodically bonded structures. Shifted threshold voltages [3], increased interface trap density [4], and increased leakage currents [5] of devices have been reported in earlier studies. This poses a potential problem to packaging electronics and MEMS by anodic bonding.

We have investigated the electrical degradation caused by anodic bonding, using Metal-Oxide-Semiconductor (MOS) capacitors as test structures.

EXPERIMENTAL

Silicon wafers with MOS capacitors were bonded to Corning #7740 (Pyrex) glass wafers with cavities that enclosed the capacitors. Some capacitors were unprotected, and some were covered with a 1 µm thick oxynitride layer, commonly applied in CMOS foundries. An example of a glass-silicon wafer stack is shown in Figure 1. Capacitors both situated outside the bonded area and enclosed in glass cavities were monitored. The distance *d* between the capacitor gate and the ceiling of the glass cavity was varied between 2 µm and 200 µm. On one glass wafer, the inside of the glass cavities was covered with aluminium that was connected to the silicon surface. The aluminium acted as a shielding electrode, removing the electric field across the cavity during bonding. After bonding, the cavity tops were sawn off allowing measurements of the enclosed capacitors. The effective oxide charge (N_{eff}) and the interface trap density (D_{it}) were calculated from high frequency and quasi-static capacitance-voltage measurements as described in [6]. The concentration of mobile ions (N_m) was measured by the Triangular Voltage Sweep method [6].

RESULTS AND DISCUSSION

Figure 2 shows typical increases in N_m, N_{eff}, and D_{it} for unprotected capacitors at each location of Figure 1. In the capacitors outside the glass, ΔN_m was larger than ΔN_{eff}. It is likely that the mobile ions were responsible for the measured increase in ΔN_{eff}. Ionic contamination has also been proposed to induce D_{it} [6], meaning that ΔN_m could account for the increase in D_{it} too. For the capacitors situated within glass cavities, ΔN_m can not be the origin of ΔN_{eff} and ΔD_{it} since $\Delta N_m < \Delta N_{eff}$ and $\Delta N_m < \Delta D_{it}$. N_{eff} and D_{it} were probably induced by Negative Bias-Temperature Instability (NBTI), a mechanism that occurs in oxides subjected to high electric fields at elevated temperatures [6]. ΔN_{eff} and ΔD_{it} were smaller in the capacitors with d=200 µm than in those with d=2 µm because the electric field was lower across those cavities. On the capacitors that were protected by an oxynitride layer, no increase in N_m was observed. All parameters N_m, D_{it}, and N_{eff} remained stable at the initial values on the capacitors that were protected with oxynitride and bonded to a glass wafer with aluminium shielding electrodes.

N_m values above 10^{10}cm^{-2} are not acceptable in modern electronics [7]. D_{it} values in the high 10^{11} eV^{-1}cm^{-2} range and N_{eff} values around 10^{12} cm^{-2} may also cause device malfunction, especially if the values are changed non-uniformly across the electronics chip. Hence, protection is required for electronics to withstand anodic bonding.

CONCLUSION

Packaging of electronics by anodic bonding is feasible if appropriate protective measures are taken. We recommend an oxynitride layer to prevent contamination by mobile ions. If the electronics is situated within a glass cavity, the electric field across the cavity should be reduced either by using a metal shielding electrode or by applying a cavity with large *d*.

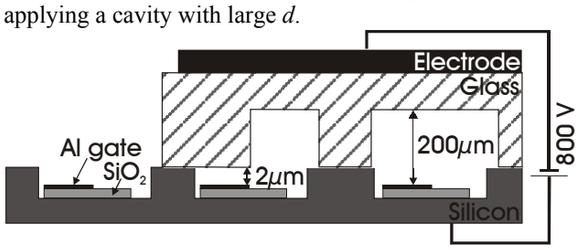

Fig. 1:A silicon-glass wafer stack with MOS capacitors at three different locations: a) is outside the glass, b) is within the glass with d = *2 µm, and c) is within the glass with* d = *200 µm.*

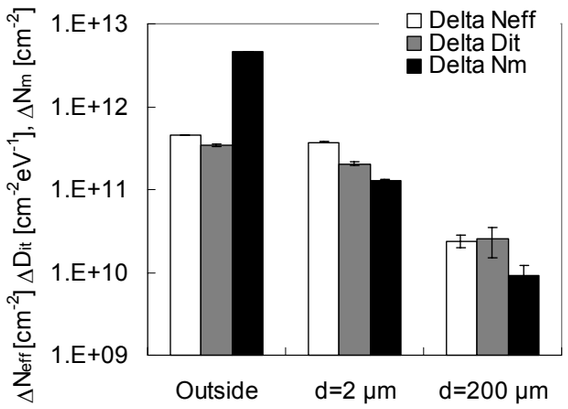

Fig. 2: The increments in N_{eff}, D_{it}, and N_m due to anodic bonding in capacitors situated at the different locations drawn in Fig. 1.

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