Development of an UHV Wafer Scale Surface Activated Bonding Machine for MEMS Packaging

M. M. R. Howlader, H. Okada, T. Itoh, and T. Suga
Research Center for Advanced Science and Technology,
The University of Tokyo
4-6-1 Komaba, Meguro-ku, Tokyo 153-8904, Japan

The key issues of packaging for micro electro mechanical systems (MEMS) devices are the alignment precision, high cost, high-density interconnection, hermetic-sealing and high temperature bonding. Current technology is not mature enough to overcome such difficulties of MEMS packaging. In order to achieve better MEMS packaging, we have developed a wafer scale robot controlled surface activated bonding (SAB) machine. SAB is defined as a fabrication process in which two solid surfaces are atomically cleaned by an energetic Argon ion beam in an ultra high vacuum (UHV) at room temperature. As a result, strong adhesion develops between atoms of the cleaned surfaces under intimate contact. The article reports on the development of a wafer scale robot controlled SAB machine and its application.

Fig. 1 shows the schematic diagram of a wafer scale robot controlled SAB machine. It consists of a transfer chamber surrounded by a processing, a analyzing, a heating, a turning over/preliminary alignment (pre-alignment), an alignment/preliminary bonding (pre-bonding), and a bonding chambers. The SAB machine can accommodate up to 8 inch wafers. An additional low vacuum chamber, called a plasma cleaning chamber in which Ar, O and H plasma treatments are possible, is also joined to the load lock chamber. The pressure ranges from $10^{-5}$ to $10^{-7}$ Pa in all chambers.

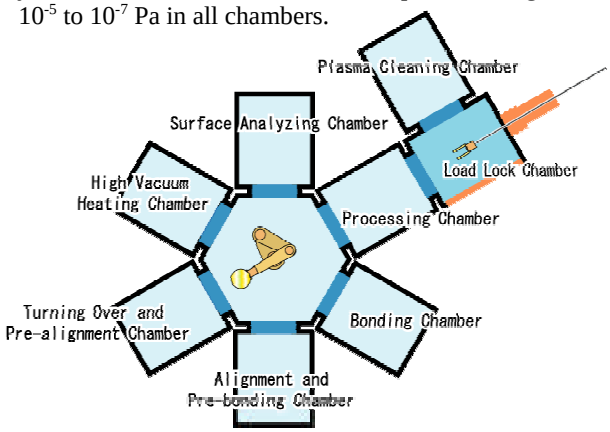


Figure 1. Schematic diagram of a robot controlled 8 inch wafer scale SAB machine.

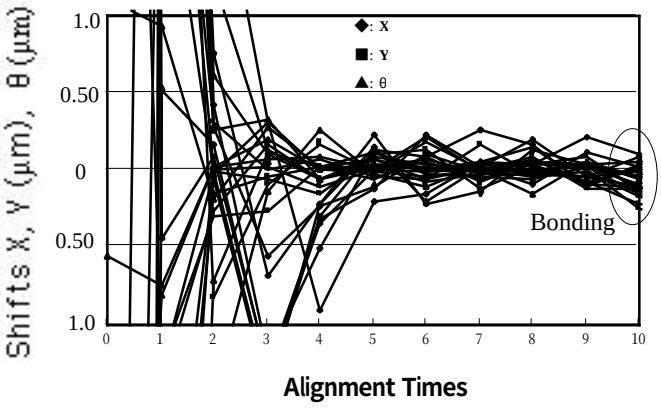


Figure 2. Alignment accuracy of the SAB machine.

Fig. 2 shows the data for 8 measurements obtained from repeated 9 times alignment of the top and bottom wafers using the Piezo Walking Table, starting with a shift of approximately 100 μm on X, Y, and θ, respectively. Two 140 mm-pitch alignment marks are used on the bottom side of upper and on the top side of the bottom 8-inch wafers. After being loaded into the alignment and pre-bonding chamber, the top and bottom wafers are rectified to less than ±0.5 μm of displacement for X, Y, and θ by the Piezo Walking Table. The bonding head comes down to bond the top and bottom wafers with applying a load of 500 N on the 8 inches wafers. Pre-bonded wafers can be cold rolled under a load up to 10000 N in the bonding chamber.

Samples were sputtered in the processing chamber by a low energy Argon ion beam with a voltage of 80 V and an amperage of 3 A. The sputtering time for Si/structured Si, Si/Au/fused silica, and Quartz/Quartz were 5, 10, and 30 min, respectively. The sputtering was done in such a way that the sample surfaces were free from contaminants but contain a non-visible amount of Fe. Si/Au/fused silica, and Quartz/Quartz bonded wafers annealed at 573 for 8 hr and 773 K for 1 hr, respectively. Si/Si bonded wafers were not annealed. Bonded wafers were cut into small pieces and subjected to tensile test. Bulk fracture was obtained in all samples with bonding strength ranges from 6 to 23 Mpa depending on the sample types.

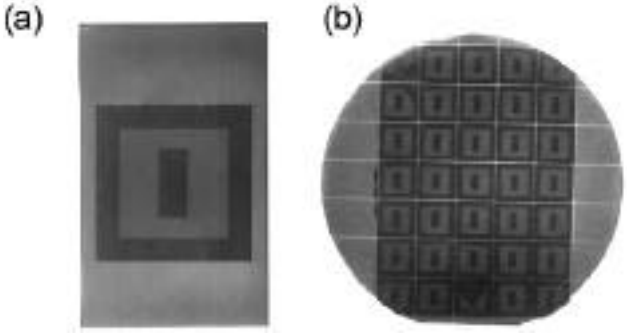


Figure 3. Infrared transmission images of Si/Si cavities used in fine leak test.

Fig. 3 shows the infrared images of the cavities formed after bonding between bare Si and structured Si wafers. The estimated leak rate of such cavities was less than $1.0X10^{-12}$ Pa $m^3/s$, which satisfies the requirement of $1.0X10^{-9}$ Pa $m^3/s$ for MIL-STD-883E encapsulation standard. Figure 4 shows the high-resolution TEM image of Quartz/Quartz interface. An amorphous layer of 100 nm is observed across the interface. No Fe is detected by EDS analysis. In addition, no substantial effect of Fe on the ultra-violet transparency and reflectance of 30 min irradiated Quartz wafer surface. Inhomogeneous growth of dendrites across the interface of Si/Au/fused silica is observed due to the diffusion of Au in Si (not shown).

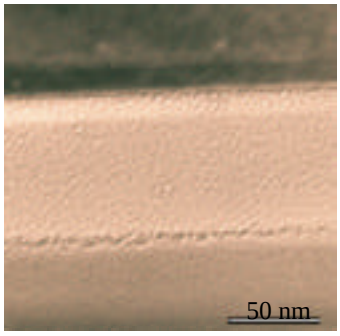


Fig. 4. HRTEM image of Quartz/Quartz interface.