Characteristics and Applications of Silicon Direct Bonded Interfaces.

P. McCann[1], Claire Devine[1], H.S. Gamble[2], W.A. Nevin[1]
[1]Analog Devices Belfast
5, Hannahstown Hill, Belfast, BT17 0LT, N. Ireland.
[2]Queen's University of Belfast, Ashby Buildings,
Stranmillis Road, Belfast, BT7 1NN, N. Ireland.

Silicon on silicon fusion bonded substrates are an ideal replacement for epitaxial deposition in the manufacture of high power devices due to lower cost and better thickness control. This allows silicon wafers to be manufactured containing several layers of single crystal silicon. These layers can have doping ranges from 10,000ohmcm n-type to very highly doped implanted regions. A high quality wafer can be produced with low warpage and a low defect density with a small thickness deviation in the substrate. The bonding process allows the use of different silicon orientations and different thermal budgets to achieve the required profile. This process is also ideal for photo-detectors, where silicon quality and thickness control are important for maximizing device efficiency.

Silicon on silicon bonding is widely used for production of MEMS devices including pressure, rate and position sensors. Wet or dry etching prior to bonding can form cavities and a combination of differences in orientation and doping levels enables novel release structures to be realized. The concept of multi-layer bonding can give additional capability for fabricating novel MEMS structures.

In this work we have investigated the influence of annealing temperature, crystal orientation, and material type on the electrical properties of the bonded substrate. The variation of process flows to form etched structures for the fabrication of MEMS devices is discussed. Silicon on silicon substrates are formed by hydrophobic cleaning of the silicon surface and bonding, followed by high temperature annealing. Silicon CMP is used to thin the layers and achieve a TTV of +/-0.5um.

The PIN diodes were 350um N+ silicon wafer bonded to a <111>, N-, intrinsic layer, with a 3um P+ diffusion. PN diode structures with a 5um N- 14ohmcm layer bonded to a handle layer of the same material were fabricated to test the bonded interface. Electrical characterization involved I-V profiles of the diodes in forward and reverse bias. Physical characterization entailed Spreading Resistance Profiling (SRP), Transmission Electron Microscopy (TEM), and Secondary Ion Mass Spectrometry (SIMS). In order to highlight the effects of the bonded interface PN diodes were manufactured on low resistivity material and compared to control devices on the same resistivity material

This work gives a physical and electrical characterization of the silicon direct bonded substrate and its suitability for IC devices. The effect of bond anneal temperature and orientation on the properties of the silicon for device manufacture will be discussed. The work also demonstrates novel process flows to fabricate simple MEMS structures.

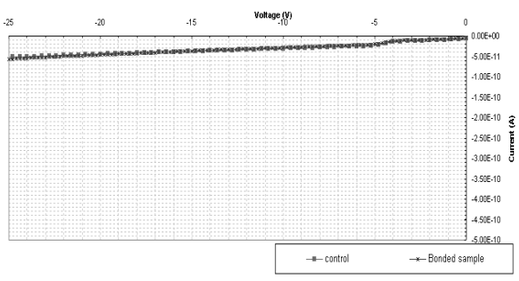

Fig 1.1 Reverse bias I-V plot comparing PIN diodes on bonded substrates to control wafers.

Fig 1.2 Simple cavity bonded layout

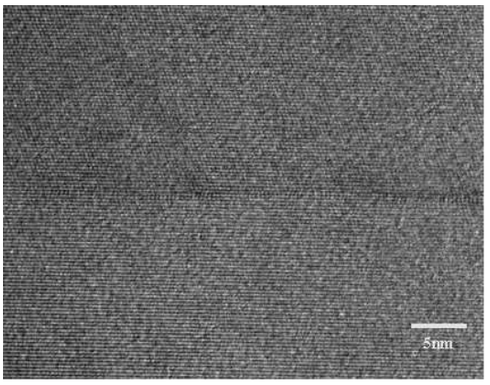

Fig 1.3 High resolution TEM of bonded Silicon-silicon interface.