WAFER BONDING IN 'STRAINED SILICON': OPPORTUNITIES AND CHALLENGES

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Tensile strained silicon layers with strain in the order of 1% show enhanced electron and hole mobilities. 'Strained silicon' technology for advanced CMOS has been announced by major companies since further down-sizing of transistor gate widths becomes increasingly difficult.
Different approaches are currently optimized that all utilize plastically relaxed SiGe as a template for strained silicon epitaxy. The most prominent ones based on chemical vapor deposition (CVD) are:

1) graded SiGe buffer layers. The Ge content in the SiGe alloy is increased with thickness in steps or linearly and relaxation of >95% is achieved in layers of several micrometer thickness /1,2/.
2) ion implantation and annealing buffer (IIAB) layers that were pioneered by Mantl et al. /3/. These buffer layers utilize He^{+}-ion implantation through a <500nm pseudomorphic SiGe layer to trigger its relaxation upon annealing at elevated temperatures (>700°C) for more that 0.5hrs /3,4/.

All SiGe virtual substrates still have high densities of threading dislocations (10^{6} - $10^{8}cm^{-2}$, depending on the composition) that all thread through the strained silicon layer and that may in addition glide in the SiGe/strained Si interface as a misfit dislocation segment before threading to the surface. These misfit dislocation segments may easily short source and drain of a transistor. All virtual substrates for bulk CMOS devices need to have a SiGe layer thickness of more than ~600nm to safely separate the interface that contains the misfit dislocations from the active device regions.
Bonding allows for different virtual substrate structures compared to bulk. Either relaxed SiGe can be bonded to an oxidized Si-wafer to be used as a virtual, so called SGOI substrate, for subsequent strained silicon channel growth or strained silicon can be bonded directly to the oxidized Si wafer (SSOI). Fig 1 shows the bonding scheme for relaxed SiGe buffer layers. Fig. 2 shows the bonding scheme to obtain SSOI. The two major advantages of bonded material are:

1) Relaxed SiGe layers with <<600nm layer thickness can be used. These layers do not contain the misfit dislocation network at the Si/SiGe interface. They may however, contain a SiGe/strained Si interface with misfit dislocations .
2) The strained silicon that is directly bonded to the oxidized Si wafer does not have any interface with misfit dislocations (Fig. 2).

Challenges in strained silicon wafer-bonding are associated with the fact that huge strains are involved in silicon and SiGe that may give rise to relaxation through processing and patterning. In this paper we will address the challenges of bonding of different virtual substrates including the role of single threading dislocations and rows of threading dislocations as they occur in graded buffer layers. We will further address how misfit dislocation related surface steps that tend to pile up in graded buffer layers affect the bonding process. Concepts to control the thickness of the bonded SiGe-layer on the atomic scale will be addressed.

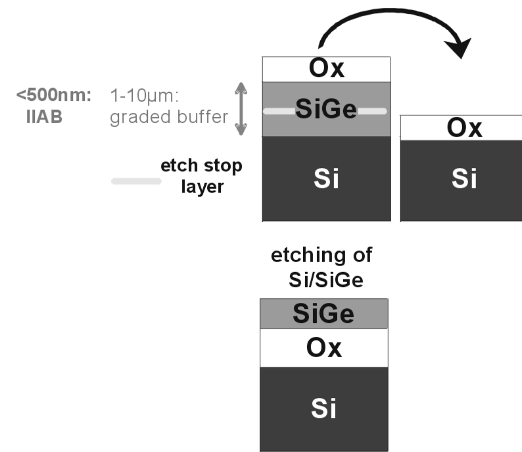

Fig.1: Bonding scheme for relaxed Si/SiGe virtual substrates to obtain SGOI.

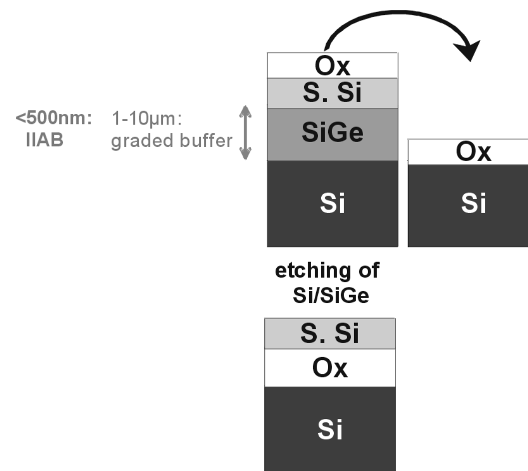

Fig.2: Bonding scheme for a strained silicon (S. Si) layer on a relaxed Si/SiGe virtual substrate to obtain SSOI.

/1/ Fitzgerald et al. J. Vac. Sci. Technol. B10, 1807 (1992)
/2/ Mooney, Mat. Sci and Eng. Rep.R17, 105 (1996)
/3/ Mantl et al. Nucl. Instrum. Methods Phys. Res. B147, 29 (1999)
/4/ Christiansen et al. Mater. Res. Soc. Symp. Proc. 686, A1.6.1. (2002)