Side gate nanotransistors by using selectively grown vertical carbon nanotubes

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The anticipated limits to the further miniaturization in size and integrity of microelectronic devices have led to increase research directed toward the development of molecular electronics. The use of carbon nanotube (CNT) has stimulated these efforts, because these molecules exhibit a range of suitable properties for nanoelectronics. The CNT, which show exceptional electronic and mechanical properties together with its nano-size diameter and hollowness, provides new model systems for basic scientific studies and pathways to nanoscale devices. Various basic single nanotube components have recently been demonstrated, such as molecular wires, diodes, field-effect transistors (FETs), [1] sigle-electron transistors, and CNT logic applications.[2] It is well established that individual CNT as a active channel of FET behave as FETs, with change in the electrical conductivity by a factor of one hundred or more under a varying electrostatic gate voltage. [3]

In this work, the selective growth of vertically aligned CNT and its application to the side gate vertical CNT-FET are demonstrated. Vertically aligned CNTs were selectively grown on the nanoholes, [4] which are formed on the anodized aluminum oxide (AAO) template fabricated by two-step aluminum anodization. The length of CNTs grown in AAO template was precisely controlled from changing the pore depth of template different from that of the CNTs grown by using CVD and dispersion by sonication. Scanning electron microscope (SEM) images of vertically aligned CNTs grown in the patterned nano pore are shown in Fig.1. The each metal electrode elements are formed on a vertical carbon nanotube attached to a bottom (source) and upper (drain) electrodes. As shown in Fig.2, the source-drain current I through the CNTs was measured as a function of the temperature. The current-voltage (I-V) characteristics of CNT show non-linear behavior with respect to temperature, suggesting the highly disordered nature of CNT. The Schottky contact model is used to explain the measured I-V curve, which shows that the Schottky barrier is estimated to be about 0.6 V at low bias voltage. We have fabricated CNT-FETs in a conventional metal-oxide-semiconductor field-effect transistor (MOSFET) structure, with side gate electrodes nearby the conduction channel separated from the channel by a thin dielectric. The Schematic image of side gate CNT-FET showing the gate, source, and drain electrodes is shown in Fig.3. These devices of the side gate geometry exhibit the effective potential distribution from the side gate electrode to the conduction channel of CNT, which is a significant improvement relative to previously reported vertical CNT-FET of top gate geometry. [5, 6] With applying a voltage to a gate electrode, the vertical CNT-FET shows ON/OFF switching operation. In this presentation, we will report simulation result and operation of vertical CNT-FET in side gate geometry in detail.

References

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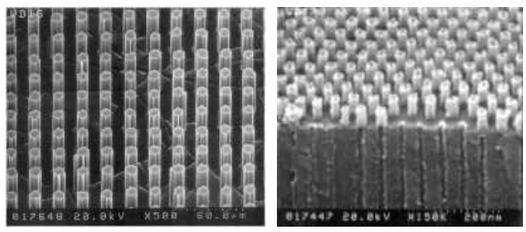

(a) (b)

Fig.1.(a)Cross sectional view of three-dimensional nanotube blocks or towers grown selectively on 5 μm by 5 μm pattern. (b) Scanning electron microscope image of vertically aligned CNTs grown in the patterned nano pore. [5, 6]

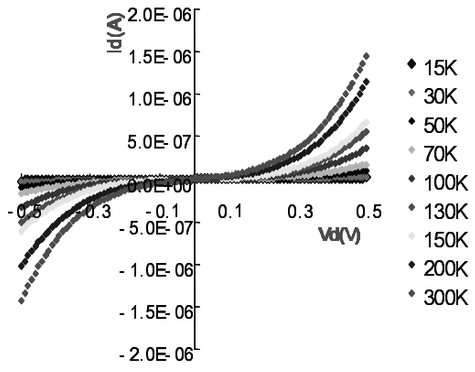

Fig.2. I-V characteristic of the vertical CNT as a function of the temperature

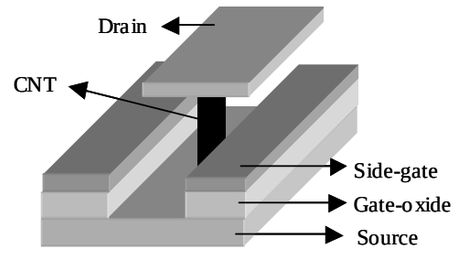

Fig.3. Schematic image of the side gate CNT-FET showing the gate, source, and drain electrodes.