

**The self-organized growth of low-resistivity NiSi quantum dots arrays by misfit dislocations on epitaxial  $\text{Si}_{0.7}\text{Ge}_{0.3}$**

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**Abstract**

As devices dimensions scale down to deep sub- $0.1\ \mu\text{m}$  size regime, self-assembly is an attractive nanofabrication technique because it provides the means to precisely engineer structures on the nanometer scale over large sample areas. Self-organizing nanocrystal assemblies have already shown the degree of control necessary to address the challenges of building nanometer-scale technologies. The fabrication of dot arrays of nanometer dimensions has attracted growing interest due to their utilization in several kinds of nanodevices. For the application of the nanodot arrays, control of the size and site of each dot is essential to optimize the properties of the devices obtained.

$\text{Si}_{1-x}\text{Ge}_x/\text{Si}$  heterostructures are used to fabricate high speed transistors that extend the range of applications of Si technology. On the other hand, the relaxed SiGe thin films can be used as templates to control the nucleation of NiSi on  $\text{Si}_{1-x}\text{Ge}_x$  alloys. For metallization in advanced devices, NiSi provides excellent properties as a contact material due to its low resistivity, low silicon consumption, low processing temperature, relative insensitivity to the linewidth of the silicide, and is well established in silicon technology. The fabrication of self-organized low-resistivity NiSi quantum dot arrays

by strain field of a misfit dislocation network has been achieved. Results of the characterization using transmission electron microscopy (TEM) and energy dispersion spectrometer (EDS) are presented.

The use of the  $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$  heterostructures template will enhance highly ordered alignment of 10-20 nm NiSi dots and create almost nano-dispersed, equally spaced nanostructures through self-organization on  $\text{Si}_{0.7}\text{Ge}_{0.3}$  with a periodic strain-relief pattern. The process promises to be applicable in fabricating future nanoscale high-speed  $\text{Si}_{1-x}\text{Ge}_x$  devices.