# Electrical Measurements of Thermal-Processed CVD-Si/SiGe Layers on Nanometer-Thick SOI

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**Introduction -** SiGe is an interesting material to develop future electronic devices. SiGe-channel PMOSFETs on SOI (Silicon on Insulator) have the attractive characteristics such as small subthreshold swing, mobility enhancement, and suppressed short channel effects. The device performance greatly depends on the quality of Si and SiGe epitaxially grown on a SOI substrate. It also depends on the Si thickness of SOI – the thin Si is required. We have demonstrated that an LPCVD method using ultraclean technique is very useful in growing dislocation- and contamination-free SiGe wells with the abrupt hetero-interfaces.[1-3] In this report, we grew Si/SiGe/Si layers on the nm-thick Si of SIMOX (a silicon-on-insulator substrate formed by the technique of Separation by IMplanted OXygen) and formed PMOSFETs on the layers.[4] The device fabrication process included 800℃ heat-treatment. The purpose of the work is to investigate the quality of the device-processed layers by electrical measurements.

**Experimental Procedure -** The (100)-oriented SIMOX wafer with the SOI thickness of 283 nm was etched to the 7- or 21-nm-thick SOI with dilute HF solution. The wafer surface was rinsed with RCA solutions and etched with dilute HF solution just before loading into the LPCVD reactor. The substrate temperature was kept at 550℃. The source gases were $Si_2H_6$ and $GeH_4$ and the carrier gas was $H_2$. The total pressure during growth was 1-3 Torr. Si buffer layer, 13-nm-thick SiGe layer with the Ge composition of 20 % and 7-nm-thick Si top layer were grown on the wafer surface. The 5.9 nm gate oxide film was formed in dry $O_2$ at 800℃ for 60 min. The source and drain regions were formed by $BF_2$ ion implantation (15 keV, $2x10^{15}$ $cm^{-2}$). The channel length was at a range of 1.5-30 um and the channel width was at a range of 1.5-400 um. The highest process temperature in fabricating the devices was 800℃. I-V measurements for the devices were done at room temperature.

**Results and Discussion** – We epitaxially grew $Si/Si_{0.8}Ge_{0.2}/Si$ layers on a SIMOX wafer with the 59-nm buried $SiO_2$ layer. We found no unstrained dislocations for the as-grown and 800℃ heat-treated samples with the 283-nm-thick SOI by TEM. We fabricated three PMOSFETs (D-283, D-21 and D-7) on the layers. Table 1 shows the Si thickness of SIMOX wafer and buffer layer for the devices. Figure 1 shows the subthreshold characteristics of the devices at the $V_{DS}$ = -0.1 V. The current decay curves were almost all similar. The $V_{th}$ of D-283, D-21 and D-7 taken at the $V_{DS}$ = -0.1 V were –0.94, -0.94 and –0.89 V, respectively. The peak transconductance of the devices were 0.23, 0.20 and 0.17 mS/mm, respectively. Figure 2 shows the I-V characteristics of the D-7 device in the saturation region. The saturation current of $I_{DS}$ was 0.21 mA. The currents for the D-21 and D-283 devices were 0.24 and 0.28 mA. The results show that the current depends on the SOI thickness of the device. As is well known, the interface area between the buried oxide and SOI includes a large number of defects. For the case of D-7 device, the quality of the Si and SiGe layers was supposed to be degraded because the 7-nm-thick SOI was too thin to buffer the density of the defects.

**References**

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Table 1 Si thickness and threshold voltage of PMOSFETs

| Device | D-283 | D-21 | D-7 |
|---|---|---|---|
| SOI (nm) | 283 | 21 | 7 |
| buffer Si (nm) | 20 | 20 | 4 |
| $V_{th}$ (V) | -0.94 | -0.94 | -0.89 |

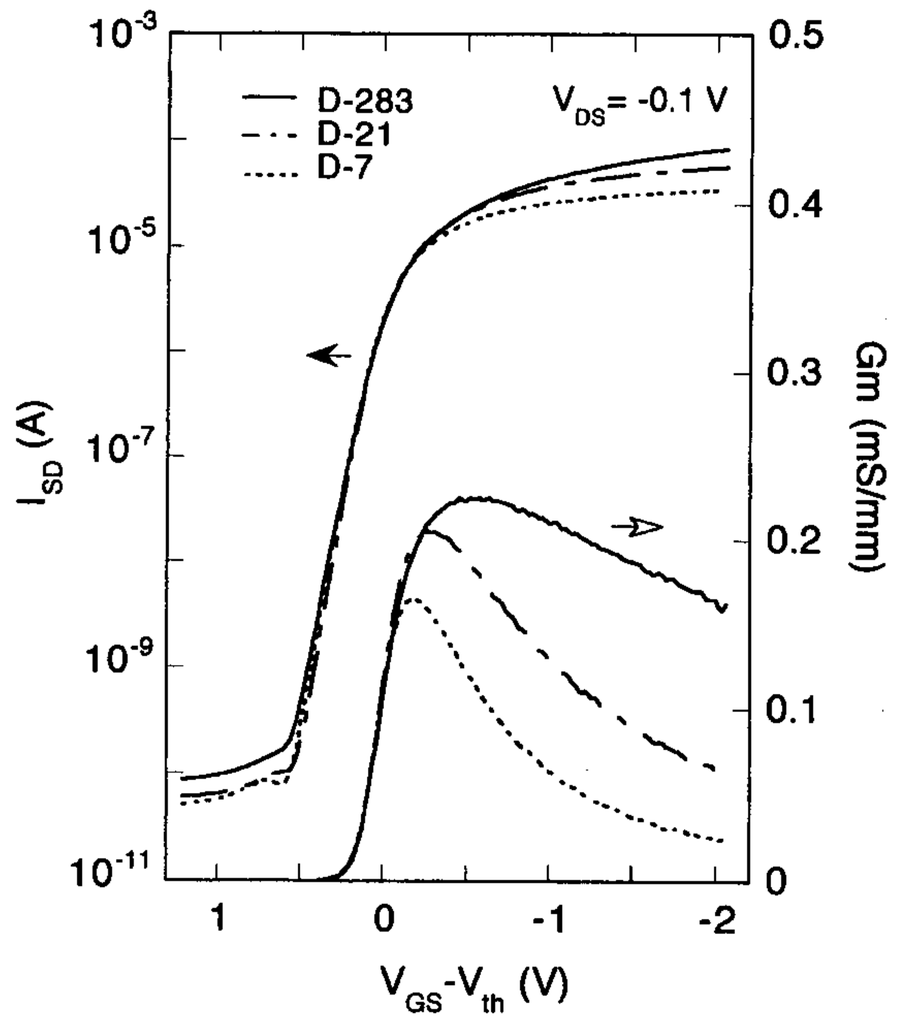


Fig. 1. Subthreshold characteristics of the devices (channel length = 10 um, channel width = 200 um)

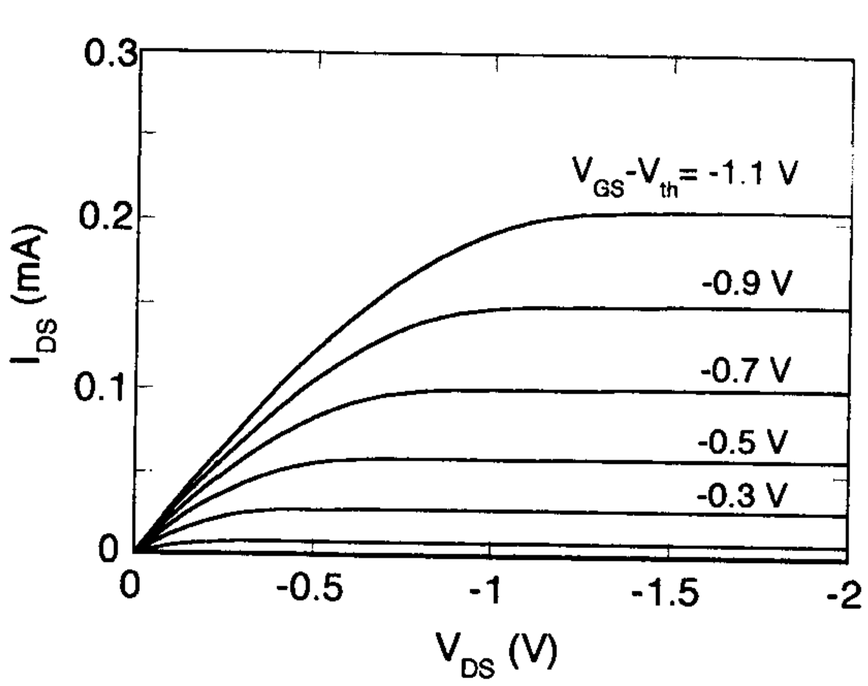


Fig. 2. I-V characteristics of the D-7 device in the saturation region