Optimizing Net Deposition Rates for a High Density Plasma CVD Process

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Silicon-oxide deposition in high density plasma CVD discharges is a commonly used process for the formation of inter-metal dielectrics during the fabrication of IC devices (1, 2). The high density plasma CVD process consists of a deposition reaction driven by the electrons in the plasma discharge, together with an ion sputter reaction, caused by the flux of high energy ions impinging on the surface of the wafer (3, 4) The ions are energized by the self-bias impressed on the wafer by an auxiliary RF power supply and therefore their energy can be controlled independently from the bulk plasma density and electron temperature. The ion sputter reaction is critical for successful gap-fill as in the absence of the erosive effects of the ions the deposited film tends to accumulate at the top of the inter-metal gaps leading to "pinch-off" and void formation. A common approach in HDP-CVD process development is to adjust the deposition and sputter rates in discrete steps during deposition to take advantage of the improved gap geometry as the CVD process progresses resulting in improved deposition rates. An obvious process improvement is to allow the deposition and sputter rates to vary continuously during the deposition process. The ratio of deposition and sputter rates (*D/S*) is a parameter that is most commonly used to characterize the capabilities of the HDP-CVD process with regards to gap-fill. By using experimental data to posit a functional form for the dependence of *D/S* vs. gap geometry an analytical description of the HDP-CVD process can be derived to allow for the optimization of net deposition rates in an HDP-CVD chamber.

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