

A Case Study in Predictive Three-Dimensional Topography Simulation Based on a Level-Set Algorithm

C. Heitzinger,^{1,2} A. Sheikholeslami,¹ J. Fugger,³
O. Häberlen,³ M. Leicht³ and S. Selberherr¹

¹Institute for Microelectronics, TU Vienna
Gußhausstraße 27–29/E360
A-1040 Vienna, Austria

²Department of Mathematics and Statistics
Arizona State University, PO Box #871804
Tempe, AZ 85287, USA

³Infineon Technologies
Siemensstrasse 2
A-9500 Villach, Austria

INTRODUCTION AND MOTIVATION

The aim of this work is to study the etching of trenches in silicon and the generation of voids during the filling of genuinely three-dimensional trench structures with silicon dioxide or nitride. The trenches studied are part of the manufacturing process of power MOSFETs, where void-less filling must be achieved. Another area of applications is capacitance extraction in interconnect structures, where the deliberate inclusion of voids serves the purpose of reducing overall capacitance [1]. Furthermore, these simulations make it possible to analyze the variations on the feature scale depending on the position of the single trench on the wafer and in the reactor.

SIMULATION APPROACH AND RESULTS

In the ELSA simulator (Enhanced Level-Set Applications), the transient movement of the surfaces is tracked by a level-set algorithm including narrow banding and a fast marching algorithm for extending the speed function suitably [2, 3]. The particle trajectories in the simulation domain are tracked via an iterative radiosity formulation. The dominating reactions paths are based on one main reacting species [4].

Figure 1 shows an isotropic etching process and Figure 2 shows the result of directional etching using chlorine, where the incoming flux is not perpendicular to the wafer surface. Figure 3 shows the deposition of silicon dioxide into a cylindrical trench, where a void is formed.

Despite the magnitude of computational resources available today, care must be taken in the choice of algorithms to achieve sensible times for three-dimensional simulations. The simulation times for a 60^3 grid on a Pentium IV computer running at 2.8GHz are between 2.77s and 47.4s for one step in the simulations shown in the figures. A whole simulation typically consists of 100 or 200 steps.

CONCLUSION

The developed three-dimensional simulator was used for optimizing the topography manufacturing steps of power MOSFETs for automotive applications. The simulator was found to be applicable to a wide range of both etching and deposition problems and to yield predictive simulations within a reasonable time frame.

REFERENCES

1. F. Badrieh, H. Puchner, C. Heitzinger, A. Sheikholeslami, and S. Selberherr, in Proc. 33rd European Solid-State Device Research Conference (ESSDERC 2003), J. Franca and P. Freitas, Editors, p. 441, Estoril, Portugal (2003).
2. J. Sethian, Level Set Methods and Fast Marching Methods, Cambridge University Press, Cambridge (1999).
3. C. Heitzinger, J. Fugger, O. Häberlen, and S. Selberherr, in Proc. 32th European Solid-State Device Research Conference (ESSDERC 2002), G. Baccarani, E. Gnani, and M. Rudan, Editors, p. 347, Florence, Italy (2002).
4. G. Schumicki and P. Seegebrecht, Prozeßtechnologie, Springer, 1991.

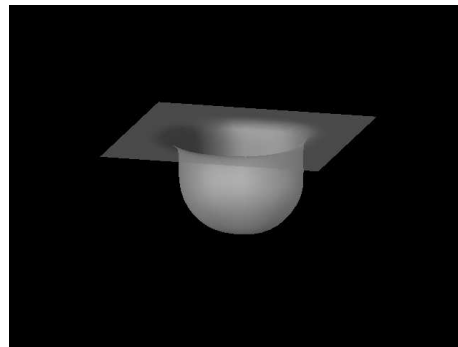


Figure 1

An isotropic etching process.

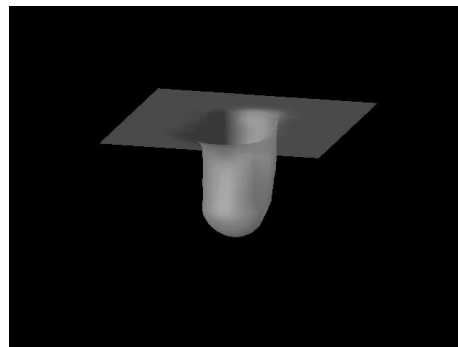


Figure 2

Directional etching.

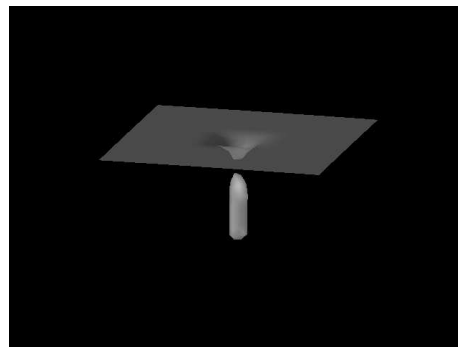


Figure 3

Starting from a rectangular trench, a deposition process results in void formation.