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PVD silver as a material of choice for microwave passives in silicon technology

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With decreasing feature sizes and increasing chip speeds, transmission delay through interconnections between active silicon devices has become a major contributing factor in circuit delay. Increased current density aggravated reliability issues. Low-k dielectrics and Cu were considered to reduce RC delay. If low-k materials for IC application are still at the development stage, all-copper interconnects are already being offered by major players in the silicon industry.

The performance of some fully-integrated circuits for communication applications, such as a voltage controlled oscillator, depends critically on the quality factor (Q) of the passive components – inductors/transmission lines. Passives with Q as high as possible are desired to reduce phase noise (PN). PN $\sim 1/Q^2$ [1]. Metal resistive losses degrade the quality factor of passives. Silver will reduce bulk resistive losses in the microwave passives to the lowest possible level. The quality factor depends also on the surface roughness. With the frequency of operation of silicon communication ICs increasing rapidly, the skin depth is shrinking. For copper with 1.8 Ω-cm resistivity the skin depth at 10 GHz is 0.66 μm [2]. When the skin layer is in the same order of thickness as the surface roughness, it is not the bulk resistivity of metal but the surface itself that defines resistive losses. Getting the metal surface as smooth as possible is important to boost Q of passives.

Silver has a room temperature bulk resistivity of 1.59 μΩcm compared to 1.68 μΩcm for copper and 2.65 μΩcm for aluminum [3]. Silver also has a high reduction potential of 0.8 V, compared to 0.34 V for copper. But Ag is susceptible to electromigration and agglomeration. This problem should be carefully addressed to validate Ag as a material of choice for ULSI back end metalisation.

Top “fat” wires in the back end interconnects are being used to build microwave passives. Electromigration is not an issue for the passives mainly because of the size of these devices. Also, with a decrease in the feature size of transistors, device-operating voltages have scaled down considerably.

Electro/electroless plating, sputtering or evaporation could be used to fabricate passives. The right choice here is important. The in-use thin-film resistivity can differ substantially from the bulk value due to impurities in the metal from deposition or from diffusion of adhesion/barrier materials.

Plating: High purity electroplated films could have 5-10% higher resistivity [3]. The lower density of plated metal and impurities, including trapped in the volume moisture and solvents, contribute to the higher resistivity. (Damascene metallization process is based on Cu electroplating. A particular problem impeding the use of plating for Cu deposition is the corrosion of copper in the presence of moister and applied bias.) The surface of electroplated metal is rough. The surface roughness of electroless plated metal is worse.

Sputtering: The higher resistivity of the sputtered films is most likely due to argon impurities in the film, if Ar was the gas used during sputtering.

Evaporation: Due to the high vacuums under which evaporation is performed, films can be deposited with very little residual gas incorporation, and thus the deposited film is about as pure as the source material [4]. The surface of sputtered/evaporated film is relatively smooth .

From all the above process options, physical vapor deposition (PVD) of silver is the obvious choice for the passives manufacturing.

In this work Cu and Ag coplanar waveguides (CPW) were fabricated and tested. Copper and silver films were deposited by e-beam evaporation onto unheated 2 inch silicon wafers of 7.3 Ω-cm resistivity. Prior to Cu (Ag) deposition, a thin layer of titanium (30 nm) was deposited to improve adhesion. The thickness of deposited Cu (Ag) was 2 μm. The base pressure of the deposition chamber was 5×10^{-7} Torr. Test devices were patterned by lift-off. The dimensions of test devices are in Table 1.

Table 1

	G, μm	W, μm	T, μm
Cu CPW	17	13	2
Ag CPW	17	13	2

S-parameter measurements were performed up to 40 GHz with a standard AC test set. SOLT calibration was used. Test devices were measured at different locations across the wafer to take into account the variations in substrate resistivity and device dimensions.

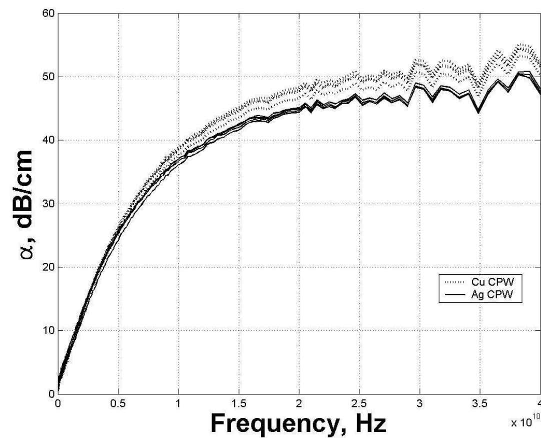

Fig.1 Measured attenuation of Cu and Ag CPWs as a function of frequency. Dotted lines are present Cu CPWs.

As can be seen in Fig.1, all test devices show high attenuation (α) because of the losses in the silicon substrate. But Ag CPWs have less attenuation than Cu CPWs, (noticeably after 10 GHz) because of smaller resistive losses in silver. The difference in attenuation for Ag and Cu devices could be estimated in 2-3 dB at 40 GHz.

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