Introduction To Nanoscale Packaging And Systems

Rao Tummala, Georgia Institute of Technology-Packaging Research Center and Zhong L. 'ZL' Wang, Georgia Institute of Technology – Center for Nanoscience and Nanotechnology
813 Ferst Drive, Atlanta, GA 30332

This presentation introduces nanoscale packaging as an important emerging technology. As the semiconductor industry approaches an historic transition toward nanoscales of 100nm and with more than 10,000 I/Os and 150 watts/chip, it is becoming clear that nano-packaging is necessary.

Nano-packaging comes at two levels: IC and systems, together leading to nano-systems in a decade. Wafer-level packaging, with materials such as solders at 20 micron pitch, fail due to poor fatigue resistance. Compliant structures, on the other hand, are expensive and have too high an inductance and electrical resistance. However, nano-interconnects provide an opportunity to have the best of both electrical and mechanical properties, in addition to low cost and at-speed test and burn-in benefits not presently available. Today's systems packaging consists of bulk dielectrics, conductors for multilayer wiring; capacitors, resistors, inductors, filters for RF; and waveguides and detectors for optoelectronics interconnections, high thermal conductivity materials and designs for heat transfer, solders with underfills for assembly. Can these be scaled down to nano-dimensions with improved properties so as to end up with systems paradigms? This reviews the status of and presents potential opportunities that nanoscience and packaging technology provide in each of the above.