

Process Integration of Highly Stable 1.25 μm^2 6T-SRAM Cell with 45nm Gate Length Triple Gate FETs

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INTRODUCTION

Continuous device scaling will be faced with a severe problem of high chip power consumption, arising from ever-increasing off-leakage currents. Recently, non-planar transistor structures such as FinFETs [1] and Triple Gate (TG) transistors [2] have attracted much attention because of their promising short channel characteristics. Circuit integrations with these structures have also been reported such as functional inverters, a 4.8 μm^2 SRAM cell with FinFETs [3] and an 1.25 μm^2 SRAM cell with TG-transistors [4]. In this work, we further advance the art by demonstrating a fully working 1.25 μm^2 six-transistor (6T) SRAM cell with 45nm gate length Triple Gate transistors. Finally, the TDDDB assessment of TG-transistors for gate oxide reliability is reported for the first time.

DEVICE FABRICATION

The starting material is a SOI wafer with an 180nm silicon layer of (100) surface orientation. The wafers were then oxidized to form a 50nm thick silicon layer. Plasma-nitrided oxide of 1.3nm thickness is grown after active definition using mesa isolation. The width and height of the active body at this step are 30 and 40nm, respectively. The gate patterning with 193nm ArF photolithography and resist trimming technique, offset spacer and source-drain extension (SDE) formation are followed by activation anneal and an optimized Ni-silicide process. The conventional 4-level Cu BEOL process completes the process flow. The test mask set for TG transistors was generated from the standard 90nm (planar) CMOS technology, and using deliberate optical proximity control, a SRAM cell was converted to the TG SRAM cell.

ELECTRICAL CHARACTERISTICS

The plasma nitrided gate oxide of EOT=1.3nm resulted in the reduction of gate leakage by approximately 1.5 orders of magnitude when compared to conventional SiO₂. At V_{DD}=0.85V, the I_{on}(n/p)=254/276 $\mu\text{A}/\mu\text{m}$ and I_{off}(n/p)=18/136nA/ μm were achieved, and the sub-threshold slope (S.S.) of 80 and 88mV/dec were obtained for nFETs and pFETs, respectively. From I_d-V_g curves, there was no evidence of a hump indicating rounded corners of the active body and the kink effect was absent which suggests the full depletion of the body.

The threshold voltage roll-off is completely suppressed down to 35nm gate length thanks to the superior short channel property of TG transistors, while S.S.<100mV/decade is also maintained down to 35nm gate length. Also, TG transistors exhibit excellent I_{off} reduction by 1.5 orders of magnitude at the same V_{TH} and L_{GATE} of the planar bulk counterpart. Finally, the TDDDB measurement at 85°C in Fig. 1 shows a highly reliable gate oxide integrity judging from the maximum operating voltage of 1.5V.

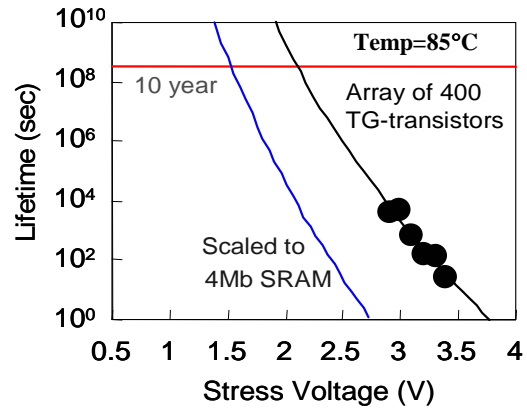
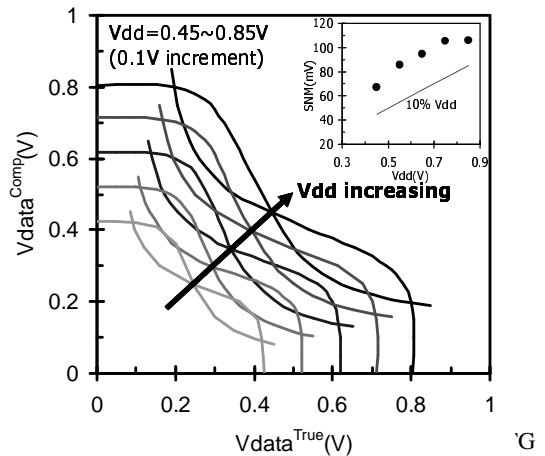


Fig. 1: TDDDB measurement results at 85°C for an array of 400 TG transistors, demonstrating highly reliable oxide integrity.

The SRAM test cell used to investigate the cell functionality consists of 6 transistor array. Robust data storing capability is demonstrated in the bi-stability curve in the wide V_{DD} range 0.55~0.85V, and the stable static noise margin (SNM) higher than 10% of V_{DD} is obtained (Fig. 2), thus indicating highly stable cell operation. Investigations into the internal node voltage behavior during write zero and read operation demonstrate that clear write zero and low node voltage disturbance during read operation are achieved.



transistors. The SNM of higher than 10% V_{DD} is obtained.

CONCLUSIONS

This work presents the experimental demonstration of a fully working 1.25 μm^2 TG SRAM cell which is the smallest cell size ever reported for a non-planar 3D transistors. The transistors exhibit excellent short channel effect control down to 35nm gate length, and possess comparable I_{off} at 150mV lower V_{TH} compared to conventional planar MOSFETs. The SRAM cell demonstrates good bi-stability for data storage, SNM values of more than 10% of V_{DD}, and reliable read/write operations. These findings clearly support the view that the TG transistors are a viable option for future generation technologies.

REFERENCES

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