Gate Dielectric Impact for the 65nm Digital and Mixed Signal Platform Applications

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Abstract

The introduction of new gate dielectrics to meet the aggressive digital specifications of future CMOS technology can have significant impact on the functioning of mixed-signal applications. In this paper, the potential of new gate dielectrics (oxynitrides, high-K) is evaluated by monitoring digital and analog key parameters of mixed-signal technology. A focus on the introduction of Plasma Nitrided oxynitrides for the 65nm CMOS technology node is presented. We demonstrate that for the 65nm node, the introduction of Plasma Nitridation benefits both digital and analog applications. The compatibility of Plasma Nitridation for implementing multiple oxides within a single chip is also evaluated.

Introduction

Mixed-signal applications of CMOS technologies are among the most complex microelectronical platforms to establish. Indeed, in case of single-chip integration, different functionalities are living together, with proper technological requirements from either analog or digital applications. Such SoC (System on Chip) has to deal with digital parts of the IC which require speed and low consumption (logic and memory circuitry) and in parallel with non-digital parts (analog circuitry) to communicate with the outside world. In general, logic circuitry represents the main part of the applications, increasing digital performances (increase speed, density, reduce power consumption) is generally driving the evolution of CMOS technologies. The introduction of new materials (oxynitrides and high-k gate dielectrics, metal gate electrodes, material for stress engineering, etc.) or architectural breakthroughs (Multi Gate transistors, FDSOI, SON, etc.) will be unavoidable to match the digital specifications of 65nm CMOS nodes and beyond. As a consequence, the operation of non-digital parts of the IC will be automatically impacted, suffering or benefiting the application type and the technological innovation. In this paper, we evaluate the impact of new gate dielectrics on the key parameters of both digital and analog applications.

On the one hand, the evaluation of digital performance can be made through speed and consumption. The speed is related to the transistor drive (Ion) current (when the transistor is ON) and the consumption is directly linked to the off-state (Ioff) current (when the transistor is OFF) and the Igate (leakage current through the gate dielectric depending on the dielectric properties). On the other hand, analog devices that are less driven by the drive current or static power are evaluated with other criteria such as transistor matching (variation between two identical neighbouring transistors), the voltage gain (gm/gd) or the LFN (Low Frequency or 1/f Noise). In addition to the impact of the gate dielectric on these parameters it is also really important to evaluate the reliability of the new gate dielectrics that are to be introduced in future CMOS nodes. In

this paper, the reliability evaluation will be based on two major criteria: TDDB (Time Dependant Dielectric Breakdown) and NBTI (Negative Bias Temperature Instability)

The gate dielectric plays a major role in the optimisation of the digital performance. The well-known SiO_2 is now reconsidered, as the dielectric thickness is scaled down and the increase of Igate becomes more and more critical. To meet the specifications, nitrided oxides or oxynitrides were introduced in the 0.12µm technology node to reduce gate leakage. Now, despite smart optimisations (nitrogen dose increase, plasma nitridation, etc.), oxynitrides tend to reach their limits at the sub-nanometer EOT (Equivalent Oxide Thickness) (Table 1) maintaining acceptable leakage level. High-k dielectrics are seriously envisaged to replace oxynitrides allowing lower leakage current for equivalent EOT. In this paper, we consider the impact of these new dielectrics in terms of both digital and mixed-signal performances and reliability. We particularly focus on the 65nm node which is the transition point between oxynitide and high-k and where plasma-nitrided (PN) oxide was introduced instead of conventional NO furnace oxynitride. In section 1, we will introduce the various digital and analog performance criteria related to gate dielectrics. Section 2 describes how these parameters are affected by the ongoing technological innovations, while section 3 describes the introduction of plasma-nitrided oxides into the 65nm technology node

1 Evaluation criteria

1.1 Digital applications

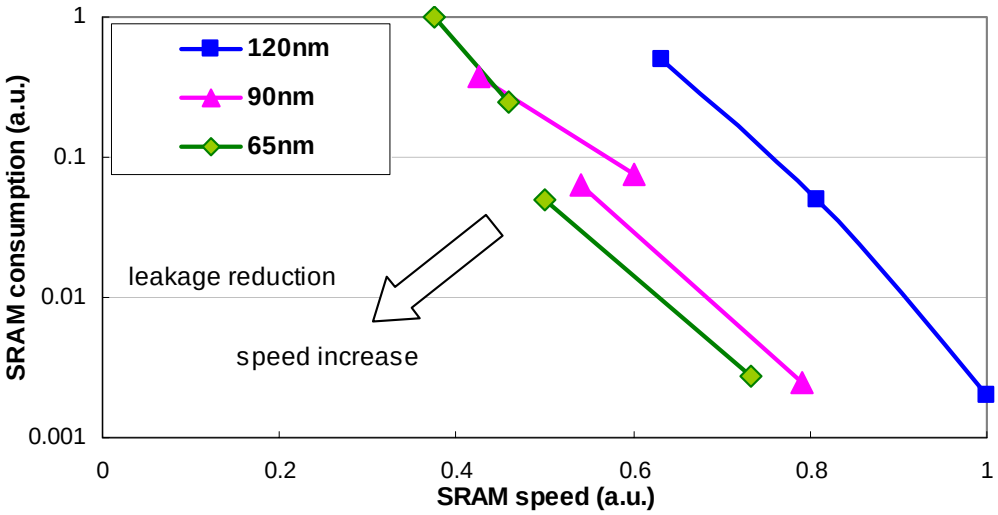

Figure 1 : SRAM bitcell consumption vs. speed for 120, 90 and 65nm.

The scaling of CMOS technology is driven by the increase of chip density, the improvement of device performances and the reduction of consumption to optimise digital applications. These improvements are influenced by key parameters such as speed, and consumption. Indeed speed is the critical driver for interactivity and multimedia electronics, whereas low power consumption is the key point of mobile and wireless applications. Figure 1 shows the trends of the 120, 90 and 65nm technology nodes for the speed of an SRAM cell and for its static consumption. One can see that the newest

technology node aims for improvement over the previous one. Leakage current issue dominates the 65nm node where it is clear that consumption and performances require a smart compromise. These two indicators are directly related to transistors parameters such as drive current (Ion) for speed, and leakage currents (Ioff and Igate) for power consumption. It is clear that Ion, partly, and Igate, entirely, are driven by the gate dielectric thickness (Figure 2, Figure 3). Moreover, Igate as a component of Ioff, can become preponderant and Ioff is then directly driven by the gate dielectric. At this point we can conclude that future technology generations require reduced EOT to maintain speed but also that leakage current must remain low to satisfy acceptable power consumption. This illustrates the importance of the gate dielectric properties in the digital functioning of CMOS transistors.

Table 1 : technological parameters and evaluation criteria used in our studies.

Drain current at Vg=Vdd: drive current Ion Drain current at Vg=0V: Ioff Gate current through the gate dielectric: Ig	
Equivalent Oxide Thickness: EOT Capacitive Equivalent Thickness: CET	Electrical thickness in accumulation regime Electrical thickness in inversion regime under Vdd (including polydepletion)
Voltage gain: g_m/g_{ds} Transconductance: g_m Output drain conductance: g_{ds}	$g_m=\delta I_{ds}/\delta V_{gs}$ $g_{ds}=\delta I_{ds}/\delta V_{ds}$
Low Frequency Noise: using α_H Hooge constant Matching: $A_{\Delta Vt}$ parameter	$\sigma_{\Delta Vt}=A_{\Delta Vt}/\sqrt{(WL)}$
Time Dependant Dielectric Breakdown: TDDB Negative Bias Temperature Instability: NBTI	

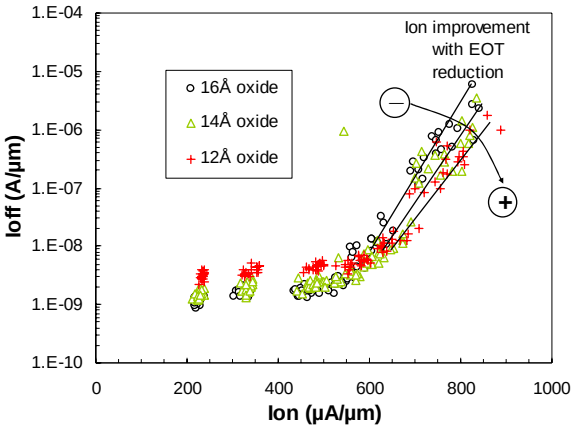

Figure 2 : Impact of the EOT on the Ion/Ioff trade-off. Reducing EOT improves the compromise, increasing the digital performances.

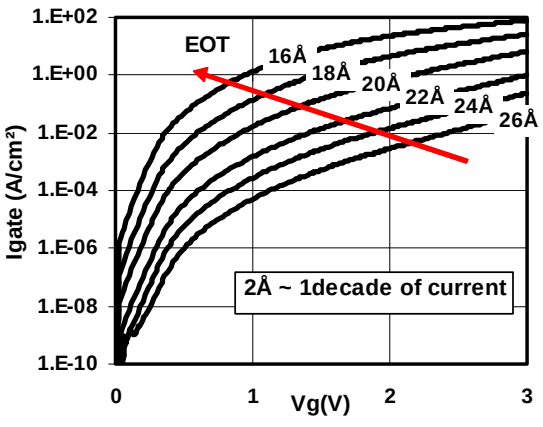

Figure 3 : Evolution of the Igate current vs. EOT for SiO_2 gate dielectric. We can assume the empirical 1decade of Igate for 2Å of EOT.

1.2 Analog applications

For mixed-signal applications, analog and digital devices are fabricated simultaneously on the same chip (Figure 14). For this reason, analog device technology

typically follows digital evolution in order to simplify integration and reduce manufacturing costs. But the aim of analog applications is more orientated to interface with the outside world, using signal treatment and transistor properties such as small signal parameters to obtain elevated voltage gain, device matching for differential stage or current mirror or low noise transistors. Matching parameter $A_{\Delta Vt}$ which corresponds to the threshold voltage variations between two identical transistors is driven by the CET (Table 1) as shown in Figure 4. We have plotted here the 1mV.µm/nm of CET rule [1] in comparison to electrical data from 120, 90 and 65nm nodes. This empirical rule was historically established on thick oxides where CET and EOT were very similar. For thin oxides, CET is more representative than EOT. We observe for 65nm node oxide, the matching is still reasonable with respect to the CET, but the general trend seems to move away from the 1mV.µm/nm of CET rule for the next generation. The same plot is represented in Figure 5 with LFN. The noise was improved from 120nm to 90nm due to a reduction of the nitrogen in the NO oxynitride, but the trend for 65nm shows that with the increase of nitrogen to reduce gate leakage, the noise level is worse than previous generations. The analog voltage gain is mostly impacted by the pocket implants used to compensate the short channel effects as shown by [2,3] One can see that all these parameters are sensitive to the device architecture and the process conditions. As a consequence, changing the gate dielectric of the digital transistor directly impacts these analog parameters which must be monitored concurrently to verify the compatibility of the new material with analog functions.

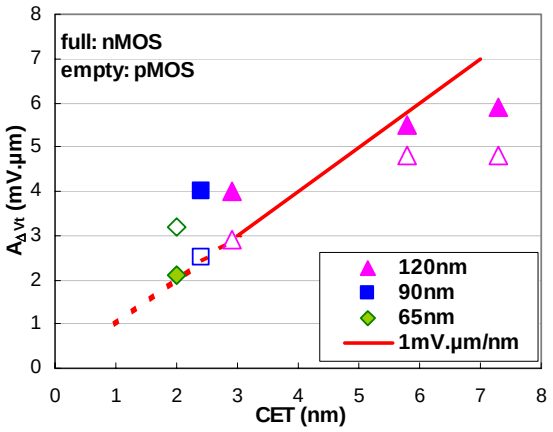

Figure 4 : Avt noise criterion vs. CET for 120, 90 ad 65nm nodes. In comparison the empirical 1mv.µm/nm of CET is also plotted.

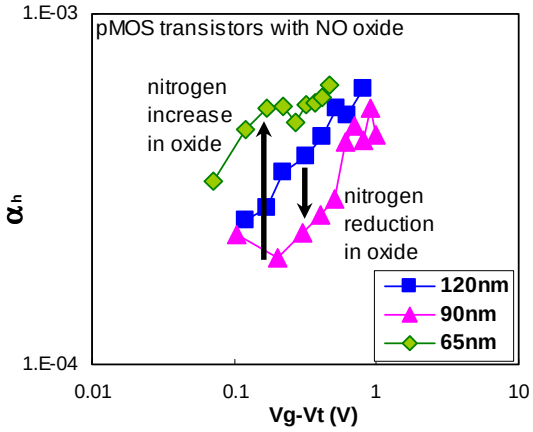

Figure 5 : Hooge constant (noise criterion) for the 120, 90 and 65nm node on pMOS transistors. The noise is driven by the nitrogen dose incorporated in the NO oxide.

1.3 Reliability

We have seen previously that the gate dielectric is one of the key points to optimise future digital CMOS devices. Assuming that a dielectric can deal with the EOT-leakage compromise, it is essential to verify the reliability of the dielectric material is sufficient to ensure acceptable life-time in the technology. In this paper, two reliability criteria will be discussed: TDDB and NBTI. Figure 6 represents NBTI data for 120, 90nm and 65nm nodes for digital applications. One can see that by reducing the EOT

with oxynitrides, we are degrading the reliability. For TDDB, reducing EOT increases the field applied on the oxide. For NBTI, in addition to the increase of the electric field in oxide, the increase of the nitrogen content also impacts the criteria (see further). For this reasons, meeting the reliability specifications will be compromised for future generations. This evidences the fact that EOT–leakage compromise and the gate dielectric must also be reconsidered in terms of reliability to match with future specifications on both digital and analog devices.

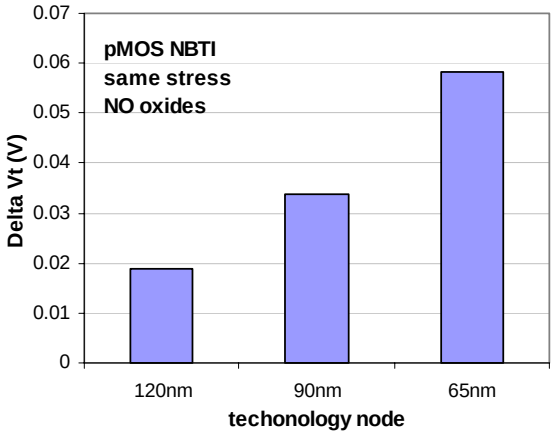

Figure 6 : NBTI reliability for 120, 90 and 65nm technology nodes with NO oxides. NBTI is sensitive to EOT reduction and nitrogen dose increase

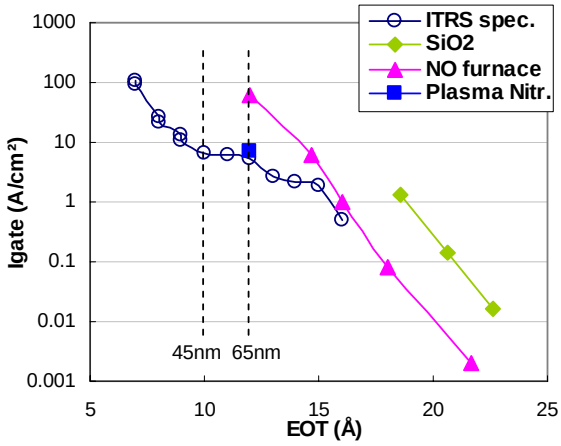

Figure 7 : Evolution of Igate vs EOT for SiO_2 and oxynitrides in comparison to ITRS specifications. The introduction of Plasma Nitridation meets ITRS for 65nm node but high-k seems inevitable for next technology node.

2 Dielectric evolutions and impacts

Figure 7 represents the ITRS specifications [4] for Igate with respect to the technology nodes. One can see that the gate leakage increase of pure SiO_2 with EOT reduction renders inevitable the introduction of new materials like oxynitrides, for the 90nm node and 65nm or heightens the needs for high-k in the 45nm node and below. Introducing nitrogen in SiO_2 permits to reduce the gate leakage but nitrogen is not free of impact for part of the evaluation criteria we presented previously. We will see that switching to high-k may also present issues on mixed-signal devices.

2.1 Increasing the nitrogen dose incorporated in SiO_2

When we talk of oxynitride we mostly consider the nitridation of a SiO_2 base-oxide under furnace NO anneal. During the nitridation, the nitrogen diffuses through the SiO_2 to reside between SiO_2 and the silicon substrate. The presence of nitrogen in the SiO_2 and at bottom interface impacts the transistor properties. The carrier mobility is influenced by this nitrogen presence but consequences to Ion current are unclear in terms of degradation or improvement [5]. However, some analog parameter degradation can be observed in LFN with the increase of nitrogen content as shown (Figure 8) [6]. We have also experimentally observed that increasing the nitrogen amount in oxynitride results in a reduction of the pocket effect (Vt roll-up) on the Vt/L profile. This phenomenon is not

well understood. This roll-up reduction leads to an increase of the voltage gain for long channel transistors as shown by [2].

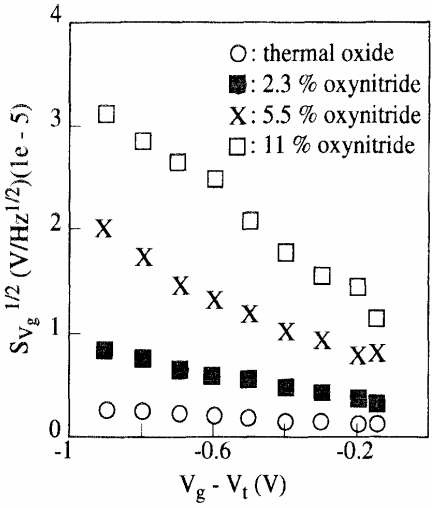

Figure 8 : Voltage noise figure for oxynitrides with various nitrogen content. The noise increase with nitrogen dose [6].

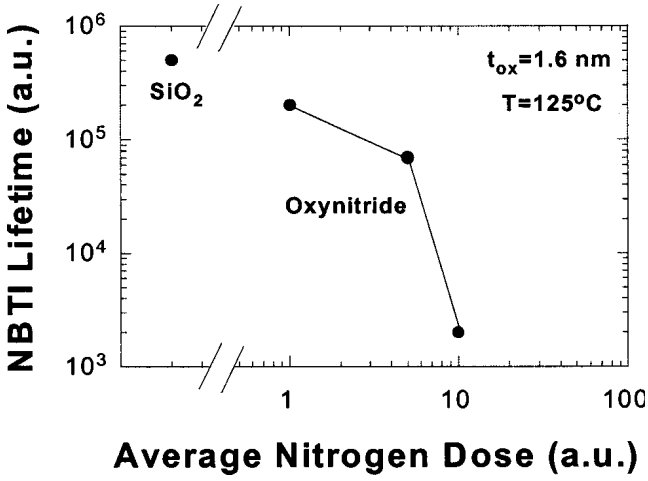

Figure 9 : NBTI life-time vs. oxynitride nitrogen content shows drastic life-time reduction with the nitrogen content increase [7]

Although TDDB is mainly impacted by EOT, NBTI is very sensitive to nitrogen incorporation and is degraded by increase of nitrogen amount as shown in Figure 9 [7]. Figure 10 and Figure 11 summarise the variation of our evaluation criteria with respect to the EOT and the nitrogen dose incorporated at the SiO_2/Si interface. As TDDB, NBTI is also degraded with the EOT reduction because of the electric field increase in the oxide.

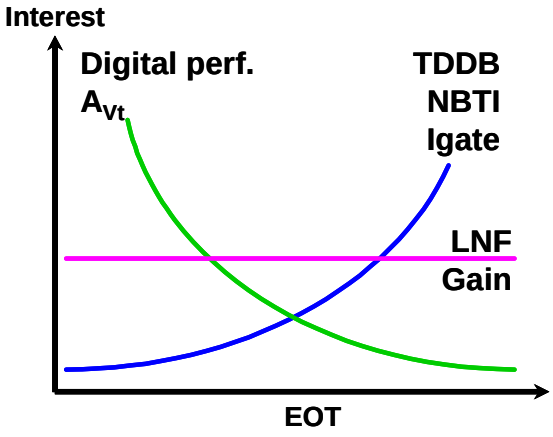

Figure 10 : qualitative interest of our evaluation criteria vs. gate dielectric EOT.

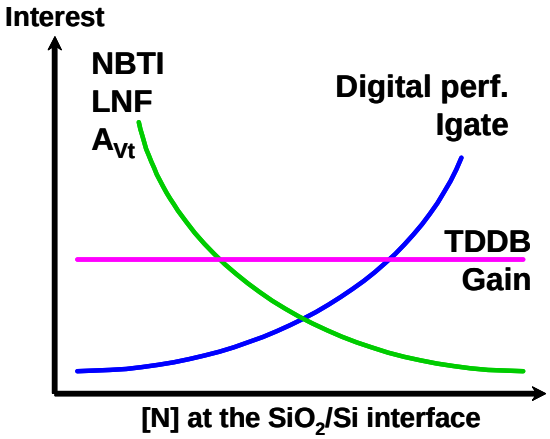

Figure 11 : qualitative interest of our evaluation criteria vs. the nitrogen content at the SiO_2/Si interface.

In order to deal with the negative impact of nitrogen, plasma nitridation was introduced. The process consists of using nitrogen plasma to incorporate it at the very top of the SiO_2 base-oxide, limiting diffusion of nitrogen to the bottom interface, allowing higher dose of nitrogen within the oxide, reducing the leakage for the same EOT. We have evaluated this technique for the 65nm node as currently under development within

the Crolles2 Alliance. The advantages of plasma nitrided oxides compared to NO anneal oxides and their impacts on mixed-signal transistors are presented in section 3.

2.2 High-k dielectrics

High-k is envisaged as the most probable solution to replace oxynitride, allowing an increased dielectric thickness while maintaining the same EOT and reducing drastically the gate leakage [8]. So far high-k dielectrics (mostly Hf-based) have posed a number of integration issues such as interaction with polysilicon gate [9], thermal stability or mobility degradation [10,11]. Now high-k dielectrics have reached an acceptable maturity and its impact even on analog applications started to be studied. For digital requirements, the mobility reduction is the main concern. For analog, the presence of charges (fixed interface as well as traps) in the dielectric is the blocking point as shown by [12]. Indeed, matching and noise are really sensitive to the interface charge density whereas mobility degradation can impact the voltage gain. However, low charge density high-k dielectrics exhibit low noise equivalent to the SiO_2 reference, see Figure 12 [13]. Moreover optimised device architectures with high-k have recently exhibited nice mixed-signal performances as presented by [14].

Concerning reliability, recent literature shows TDDB does not pose fundamental limitations, being dominated more by intrinsic effect of the dielectrics than by manufacturing-induced defects (such as charges) [15,16]. On the contrary, dielectrics trapping or fixed charges severely impact the NBTI and even PBTI criteria, increasing Vt shift degradation. However, acceptable lifetime was observed on optimised materials [17]. As for analog, the material quality is one of the key points of the high-k integration for a mixed-signal platform. The full integration and qualification of high-k materials for future technology nodes will require the high-k dielectric to approach or exceed the "historical" reference performance of oxides and oxynitrides in both the digital and analog domain.

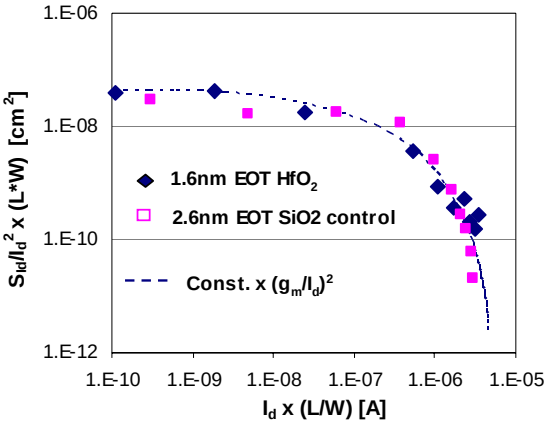

Figure 12 : Normalized spectral density of current noise *vs*. drain current for transistors with SiO_2 and HfO_2 dielectrics [13]

Table 2 : specifications for the 65nm node within the Crolles2 Alliance [18], in comparison to experimental Igate results for NO furnace oxides

		GP	LP		
	Vdd (V)	0.9	1.2	0.9	1.2
	EOT (Å)	12	18	12	18
	Lgate (nm)	45	60		
nMOS	Ig (A/cm²)	7	0.025	40	50
pMOS		7	0.005	77	10
				NO oxide	

3 65nm node: introduction of Plasma Nitridation

The 65nm node is at the transition between oxynitrides and high-k dielectrics. Indeed, if we look at the specifications we have for the core device in Table 2 [18], one can see that the conventional NO furnace oxynitride cannot satisfy the gate leakage for an EOT of 12Å with the current timelines for introducing the 65nm technology node. High-k dielectrics are perceived as not mature enough to replace the oxynitride. The introduction of plasma nitrided (PN) oxide is the solution to meet the gate leakage specifications avoiding the difficult breakthrough needed for high-k. In this part, we present the significant impacts seen on both digital and analog devices induced by the introduction on PN oxide, considering the whole 65nm platform with GP (General Purpose, 12Å EOT, mostly digital) and LP (Low Power, 18Å EOT, mostly digital) core devices as well as I/O devices (50Å EOT, digital and analog). Compatibility features of core and I/O devices are also evocated.

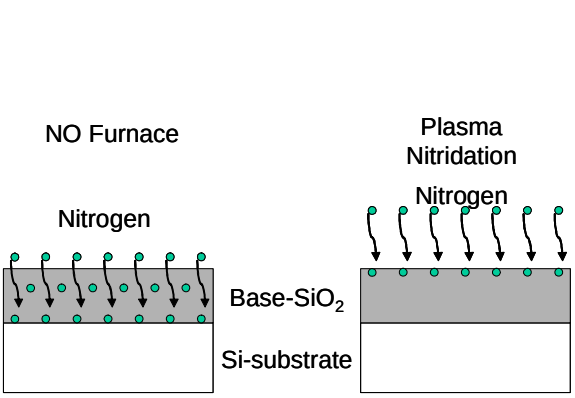

Figure 13 : Comparison between NO furnace and Plasma Nitridation oxynitrides formation. With Plasma Nitridation, the nitrogen is maintained at the top surface of the base-oxide while it diffuses to the bottom interface with the NO furnace process.

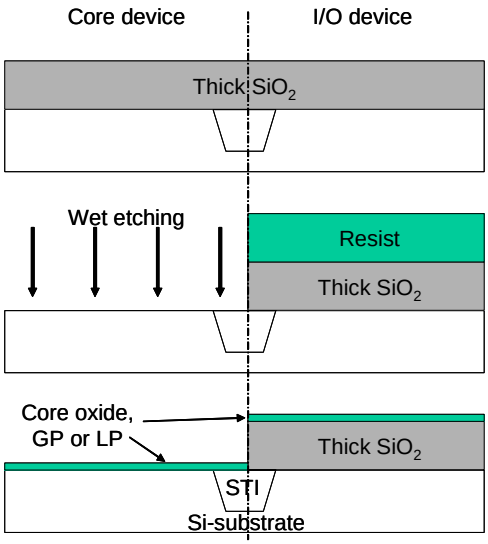

Figure 14 : process steps of core and I/O gate oxides co-integration within a mixed-signal CMOS technology. First the thick oxide is processed. After patterning, this oxide is removed on core device area. Then, thin oxide is process on both I/O and core device areas.

3.1 Core devices

In scaling down the best-suited gate oxide for 65nm CMOS, switching from NO to PN permitted to reduce gate leakage without degrading Ion current of GP devices (Figure 15). The direct consequence of this leakage reduction was the improvement of speed and consumption (Figure 16) as requested by digital applications. For analog criteria, similar matching and gain were obtained with reduced LFN level. As explained previously, the nitrogen distribution is different in PN than NO oxide, more located at the top-interface (Figure 13). As a consequence, a reduction of nitrogen-related traps (cause of noise) is observed near the silicon/oxynitride interface. Reliability of GP transistors was maintained with PN oxide [19].

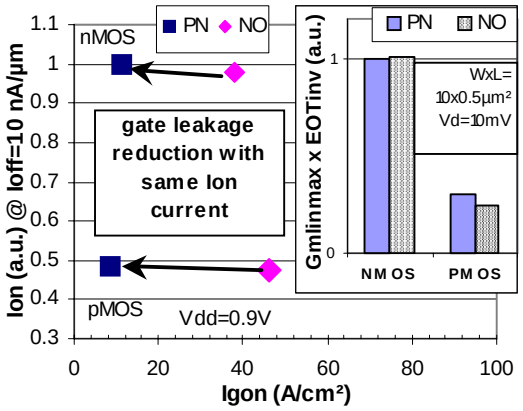

Figure 15 : Normalized Ion current vs. Igate for PN and NO oxynitrides shows gate leakage reduction with PN. Linear Gm (inset) shows similar results

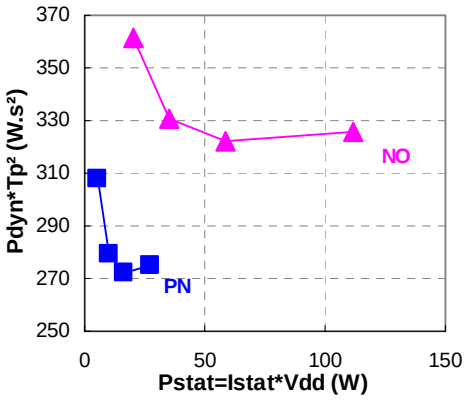

Figure 16 : Energy per transition vs static power summarizing the better behavior of PN in terms of power consumption

As far as LP devices are concerned, PN oxides exhibit similar leakage improvement for LP as for GP devices but with significant improvements for LNF, and reliability. Indeed, the PN is more efficient to maintain the nitrogen at the top interface with thicker oxides, hereby reducing the nitrogen content at the silicon/oxynitride interface. With its 18Å EOT oxide, the LP transistor is more sensitive to the noise reduction (Figure 17) than observed on GP. For the same reasons, NBTI criterion has been improved and a significant increase of the lifetime is observed on LP devices with PN with respect to NO oxynitrides (Figure 18).

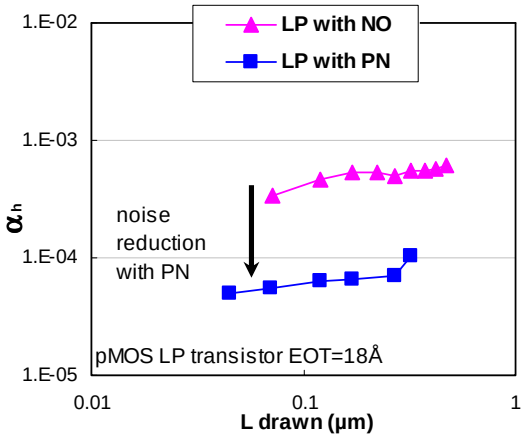

Figure 17 : Hooge constant noise criterion for pMOS LP transistors with NO or PN oxynitrides of 18Å EOT. PN devices exhibit reduced noise.

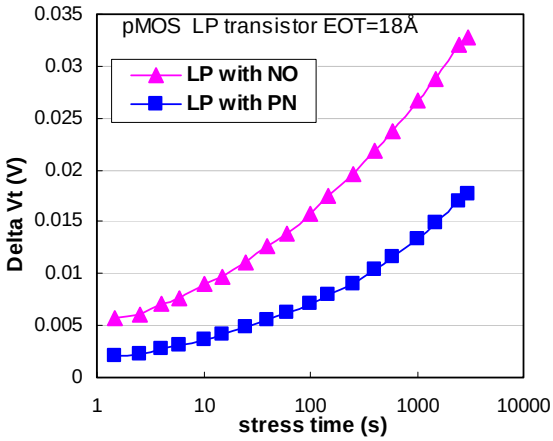

Figure 18 : NBTI (delta Vt) for pMOS LP transistors with NO or PN oxynitrides of 18Å EOT. PN devices exhibit reduced NBTI.

3.2 I/O devices

I/O devices are driven by core device architecture with very little optimisation latitude. For a strategy of mixed-signal applications, the impact of core-device changes must be verified early in the development. I/O devices require thicker oxides (50Å, for 2.5V) than core devices. In a mixed-signal technology this thick oxide is made of a first RTO SiO_2 plus the NO or PN process used for the core device oxide (Figure 14). The main difference between I/O oxide with NO or PN fits into the nitrogen profile. With NO, despite the base-SiO_2 thickness, the nitrogen diffuses through it to the silicon/oxide interface whereas for PN, the nitrogen mostly remains at the top surface of the base-SiO_2 as shown by [19, 20]. As shown previously, removing nitrogen at the silicon/oxide interface directly benefits analog parameters like noise as well as NBTI reliability. These large benefits are illustrated on Figure 19, Figure 20. Other criteria like matching, gain or TDDB are not directly affected by these changes.

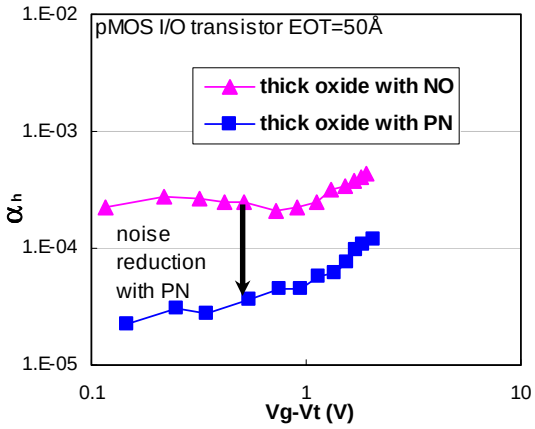

Figure 19 : Hooge constant noise criterion for pMOS I/O transistors with NO or PN oxynitrides of 50Å EOT. PN devices exhibit reduced noise

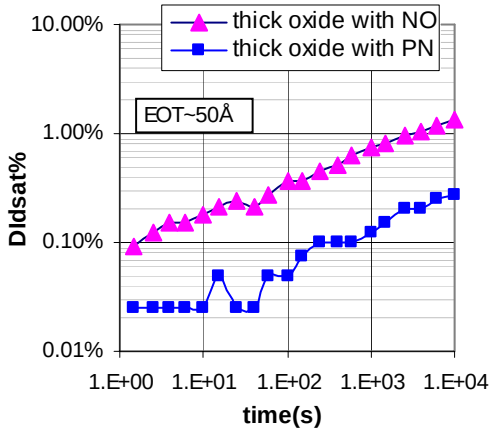

Figure 20 : NBTI (delta Idsat) for pMOS I/O transistors with NO or PN oxynitrides of 50Å EOT. PN devices exhibit reduced NBTI

3.3 Compatibility of core and I/O devices

On the level of mixed-signal design, transistor models of I/O devices must be identical for the whole technology platform. On the integration level, this means that I/O transistors must have the same behaviour whatever the core device process. Then, the impact of core device process, GP or LP, on the digital and analog performance of the thick oxide device must be carefully investigated.

In previous node (90nm), the same NO process was used for GP and LP core oxides (only the base-oxide was different). With the introduction of PN, however, different processes are used to optimise GP and LP core oxides and different nitrogen doses are incorporated within GP or LP core oxides. The resulting amount of nitrogen present in I/O oxides for the two platform variants is then also different leading to two distinct I/O devices even for the same EOT. This nitrogen dose differences impact the transistor behaviour, particularly on the threshold voltage characteristics. We have identified two issues, on nMOS and pMOS transistors that may compromise the compatibility of core and I/O devices. Figure 21 and Figure 22 present Vt versus gate

length behaviour of respectively nMOS and pMOS I/O devices for two I/O oxides made of either GP or LP PN process. One can see that for nMOS, increasing the nitrogen dose (LP process) leads to a large decrease of Vt roll-up, increasing the voltage gain of such devices (Figure 23) as previously seen. For pMOS, the threshold voltage is sensitive to the fixed charges induced by nitrogen in the dielectric leading to Vfb and so Vt shifts (Figure 22). This Vt shift should be compensated by channel doping engineering whereas additional masking for I/O device pocket implants should give latitude for nMOS Vt profiles. Unifying transistor models for both I/O devices based on GP and LP will be a key point for the compatibility of core and I/O devices for mixed-signal applications.

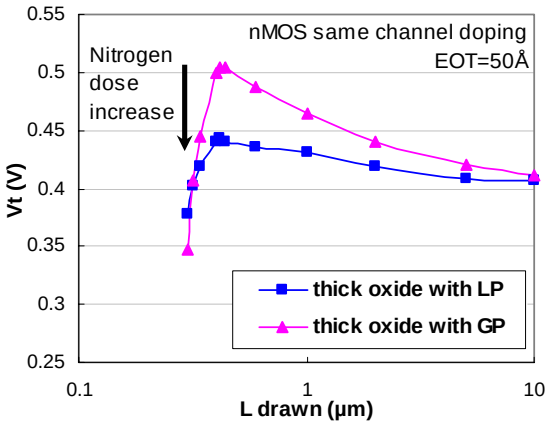

Figure 21 : Vt vs. L profile of nMOS I/O transistors with LP or GP core oxide. I/O transistors are impacted by the higher nitrogen dose with LP process, reducing the roll-up effect.

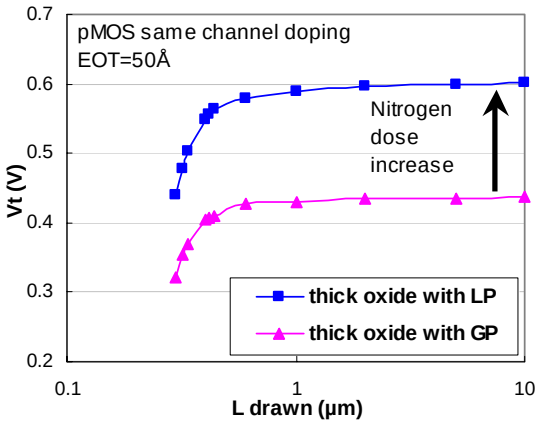

Figure 22 : Vt vs. L profile of pMOS I/O transistors with LP or GP core oxide. I/O transistors are impacted by the increase of nitrogen dose with LP process, increasing the Vt.

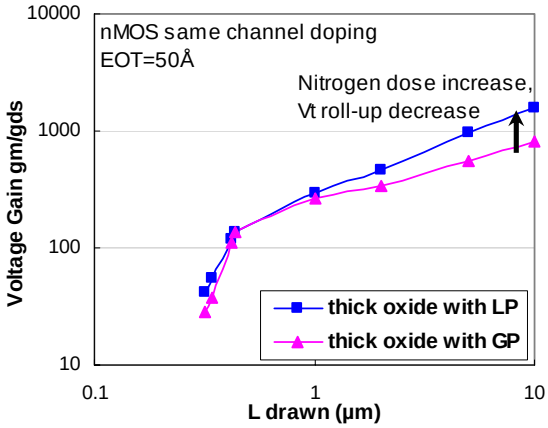

Figure 23 : Voltage gain vs. L of nMOS I/O transistors. The gain of long channel devices is improved on thick oxide with LP process due to the reduced Vt roll-up seen in Figure 21.

Table 3 : summary of the advantages and drawbacks of the PN introduction to replace NO oxide in the 65nm technology node.

NO furnace → Plasma Nitridation	
Digital perf.	=
Igate	+
LFN	+
A_{Vt}	=
Gain	=
TDDB	=
NBTI	+
Compatibility core / IO	-

In summary, we have represented in Table 3 the advantages and disadvantages of the introduction of PN process in the 65nm technology node. Apart from compatibility between core and I/O devices, that will be addressed separately, we demonstrated that PN is qualified to support conventional gate oxide processing in the 65nm CMOS

technology. All the key electrical characterization shows that PN satisfies the requirements of the 65nm platform.

Conclusions

The introduction of new gate dielectrics to meet the aggressive specifications of future CMOS technology is not necessarily detrimental for the functioning of mixed-signal applications. In this paper, we have investigated the impact of new gate dielectrics such as PN oxynitrides or high-k, on analog parameters and reliability. According to experimental results, we demonstrate that the introduction on PN oxynitride instead of NO oxynitrides in the 65nm node gives benefits to both digital and analog applications. Replacing oxide-based dielectrics with high-k materials in the future may be conceivable since recent literature data show that optimized high-k should not degrade either analog performance or device reliability. In parallel, we have shown that core and I/O device compatibility is under concern but technological compromise should solve it for the 65nm technology requirements. For next generations, with the high-k introduction, this same issue must be addressed as soon as possible.

Acknowledgments

I would like to thank all my colleagues within the Crolles2 Alliance and LETI who have contributed to this work. Thanks to all the characterisation team, particularly reliability and analog characterisation groups for their contributions and for the fruitful discussions we had. The thermal treatment team is also thanked for all the material they processed as well as for all their discussions and analyses. Finally, I would like to thanks the 65nm process integration and advanced module teams for all the support they gave on this paper. This work was partially supported by European Project MEDEA+ T207.

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