# A 65 NM CMOS TECHNOLOGY FEATURING HYBRID-ULK/COPPER INTERCONNECTS

S. Nakai, S. Fukuyama. N. Misawa, M. Miyajima,
T. Sugii, and K. Watanabe
Fujitsu Limited
50 Fuchigami, Akiruno, Tokyo 197-0833, Japan
nakai@jp.fujitsu.com

*T. Nakamura, *Y. Nakata, *I. Sugiura, and **E. Yano
Fujitsu Laboratories Ltd.
*50 Fuchigami, Akiruno, Tokyo 197-0833, Japan
**10-1 Morinosato-Wakamiya, Atsugi, 243-0197, Japan

Since 0.18 µm-node generation, we have already developed four-generation CMOS technologies featuring Cu interconnects with low-k materials (1) (2) (3). The latest technology, 65 nm node is described in this paper. For this technology, we have chosen hybrid-ULK structure which consists of NCS (Nano-Clustering Silica (4); k=2.25) at wire level and SiOC at via level. Although NCS is one of porous materials, NCS/SiOC structure has sufficient mechanical strength to endure CMP pressure and wire bondings. Hybrid-ULK/Cu interconnects fabricated at 65 nm-node design (200 nm pitch) have satisfied the electrical target from circuit requirement successfully.

References
1. Y. Takao et al., IEDM, P. 559 (2000).
2. S. Nakai et al., Symp. VLSI Tech., p. 66 (2002).
3. S. Nakai et al., IEDM, p. 285 (2003).
4. T. Nakamura and A. Nakashima, IITC, in press (2004).

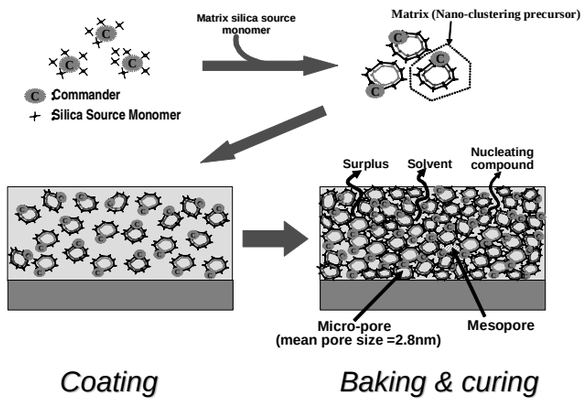


Figure 1 Unique preparation procedure for NCS film.

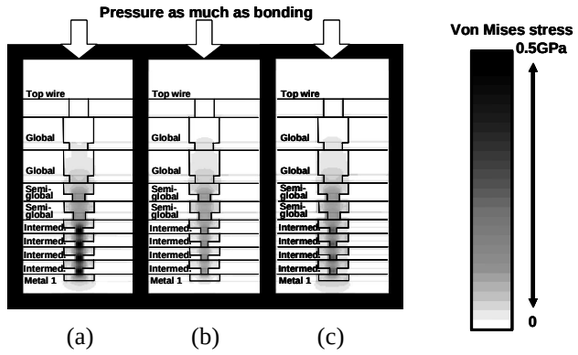


Figure 2 Simulation analysis of von Mises stress. Metal 1- and intermediate-layer dielectrics are (a) NCS homogeneous, (b) SiOC homogeneous, and (c) NCS/SiOC hybrid structure. NCS homogeneous structure has "black" areas in intermediate vias. These indicate stress-concentrated areas. SiOC homogeneous and NCS/SiOC have no black area.

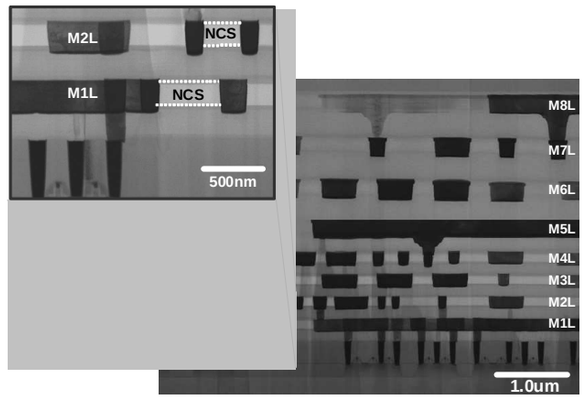


Figure 3 Cross sectional TEM image of a trial device using NCS.