DIELECTRICS IN SI NANO-DEVICES: ROLES AND CHALLENGES

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In order to improve performance and density, the size of Si MOS transistors has been scaled aggressively for more than 30 years. The physical gate length, Lgate, the most important feature size in Si MOSFETs, has been scaled by about 30% every two years. The Lgate reached sub-100nm at 130nm node in about 2001. The Si MOS transistors currently in production are at 90nm node, having Lgate of about 50nm. Research CMOS transistors with Lgate down to 10nm have already been experimentally demonstrated. Figure 1 shows A TEM cross-section of a 10nm Lgate FinFET fabricated in AMD research lab.

To solve the two major scaling issues, namely increases in transistor leakage and decrease in performance improvement, new materials and device architectures are demanded. Channel carrier mobility can be improved by inducing strain in the channel and/or by optimizing the channel surface orientation. Device designs can also be enhanced using ultra-thin FDSOI and/or additional control gates. Figure 2 shows a TEM cross-section of a 25nm Lgate triple gate FDSOI MOSFET fabricated in our AMD research lab.

Dielectrics have played and will continue to play important roles in scaling of Si nano-devices. New high-k gate dielectrics are desperately needed to control the gate leakage. Dielectrics are also widely used for minimizing parasitic capacitance, reducing channel leakage, controlling short channel effects, and inducing performance-boosting strain in the channel. Many challenges surround the introduction of a host of new materials and device architectures. Figure 3 shows a cross-sectional TEM image of nitrided Hf-silicate film sandwiched between poly-Si gate and Si channel.

In this paper, we discuss the Si CMOS fundamental scaling issues, and talk about roles and challenges of dielectrics in Si nano-devices.

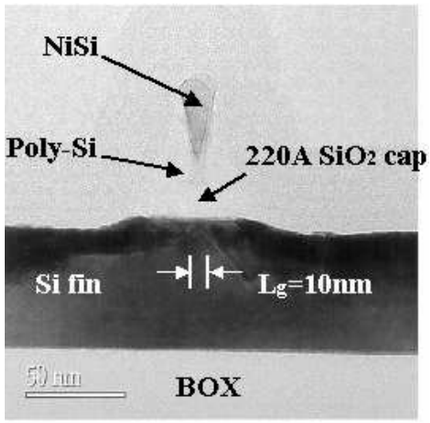

Figure 1 A TEM cross-section of a 10nm Lgate FinFET.

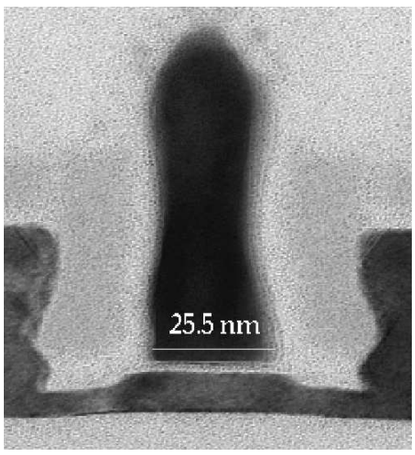

Figure 2 TEM cross-section of a 25nm Lgate triple gate FDSOI MOSFET with a N/O stack gate dielectric and a FUSI NiSi metal gate electrode.

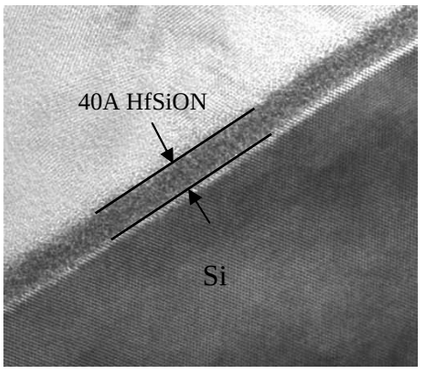

Figure 3 Cross-sectional TEM image of nitrided Hf-silicate film