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HIGH-K MATERIALS FOR TUNNEL BARRIER ENGINEERING IN FUTURE MEMORY TECHNOLOGIES

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In order to achieve 10 years of data retention, the tunnel oxide thickness in Flash memory cells can hardly be scaled below 8.5nm [1], implying the need for a very high voltage to erase (or program) the cells by tunneling through this oxide. Replacing the single layer SiO_2 tunnel oxide by a multilayer tunnel dielectric stack provides a solution combining low voltage tunneling and good data retention. [2]

At high bias, a SiO_2/high-k tunnel dielectric stack has an energy profile as shown on the right side of fig. 1. As can be seen in this figure, electrons only have to tunnel through a thin SiO_2 layer where, due to the difference in dielectric constant, the electric field is higher than the average field in the stack, leading to a high tunneling current at moderate voltage. At low bias (fig, 1 left), electrons have to tunnel through the entire stack including the high-k layer, leading to a very low tunneling probability and therefore good data retention provided that the high-k material is of sufficient quality.

We have integrated SiO_2/HfO_2 and SiO_2/Al_2O_3 tunnel dielectric stacks in single poly memory cells demonstrating fast programming and 10 years of data retention: Memory cells with 2nm SiO_2/8nm HfO_2 tunnel dielectric and a coupling ratio of 60% can be programmed by tunneling in 10µsec with a control gate voltage of 8V. As extrapolated from temperature accelerated retention tests, the same memory cells provide 10 years data retention up to 105C.

Programming of these cells is done very efficiently through the SiO_2/HfO_2 tunnel dielectric stacks but erasing of these cells has to be done in reverse direction through the same stack, therefore requiring a high electric field during a long time, quickly leading to degradation of the tunnel dielectric; Program/erase cycling is strongly limited by electron trapping in the HfO_2 dielectric during the erase operation so that only a few hundred cycles can be achieved. When Al_2O_3 is used, the charge trapping is not as severe and more than 100.000 write/erase cycles can be achieved.

Using the stack for tunneling in only one direction solves the cycling endurance problem for HfO_2. This has been demonstrated by integrating a SiO_2/HfO_2 stack as interpoly dielectric for poly-poly erase in 0.18µm HIMOS™ [3] cells. The HIMOS™ cell (fig. 3) is programmed by conventional source side hot electron injection and erased by tunneling through the SiO_2/HfO_2 stack with 3.5V on the control gate and –4V on the program gate. In this configuration, more than 100.000 write/erase cycles can be achieved without important window closure, proving that the problems observed in the single poly cell are only caused by the erase operation.

We have proposed a method for making SiO_2/high-k engineered tunnel dielectric stacks for programming or erasing of floating gate nonvolatile memory cells. Low voltage operation, good cycling endurance and good data retention have been demonstrated, partly in single poly memory cells and partly in 0.18µm HIMOS™ split gate memory cells.

References

[1] International technology roadmap for semiconductors, 2003
[2] B. Govoreanu et al, IEEE Electron device letters, vol. 24 pp. 99-101, 2003
[3] J. Van Houdt et al, IEEE Transactions on Electron Devices, 40(12):2255-2263, 1993.

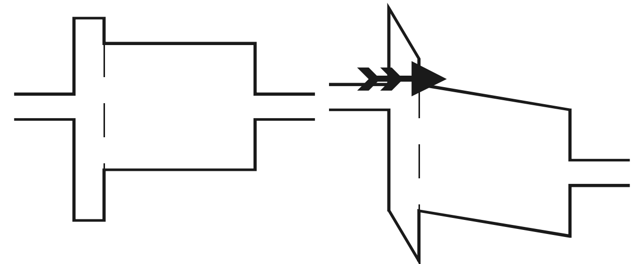


Figure 1

Band diagram of a SiO_2/HfO_2 stack when no bias is applied (left-hand side) showing a large tunneling barrier, and when a moderate voltage is applied (right-hand side) showing a strongly reduced barrier width.

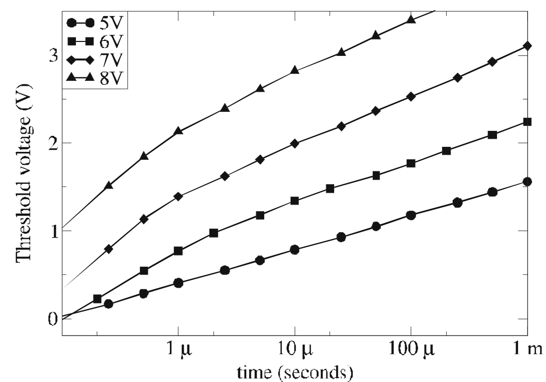
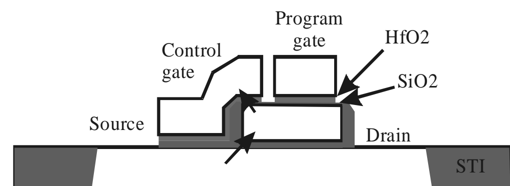


Figure 2

Programming of a memory cell with 2nm SiO_2 / 8nm HfO_2 tunnel dielectric and a coupling ratio of 60%.



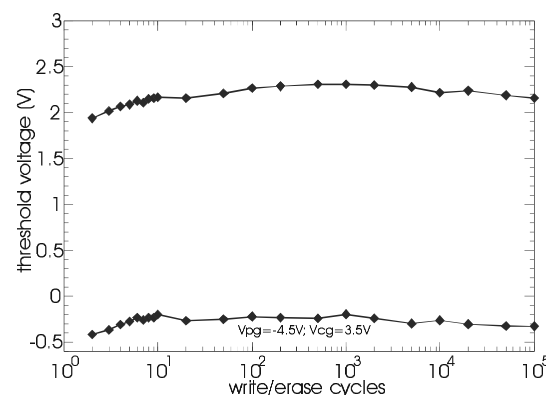


Figure 3

HIMOS™ cell structure and write/erase endurance. Writing is done by hot electron injection. Erasing is done by tunneling from floating gate to control gate through the SiO_2/HfO_2 stack.