Recent Progress in FET-type Ferroelectric Memories

Hiroshi Ishiwara

Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology
4259 Nagatsuta, Midoriku, Yokohama 226-8502, Japan
E-mail: ishiwara@pi.titech.ac.jp

1. Introduction

A key device in FET(field effect transistor)-type ferroelectric memories is a ferroelectric-gate FET, which has such features as non-destructive readout, high speed, and high packing density. However, since it is very difficult to form a ferroelectric-semiconductor interface with good electrical properties, no commercially available devices have been fabricated yet. In order to solve this interface problem, a dielectric buffer layer is often inserted between a ferro- electric film and Si substrate (an MFIS or MFMIS structure; M: metal, F: ferroelectric, I: insulator, S: semiconductor). In this structure, however, a new problem arises such that the data retention time is very short. In this paper, improvement of the data retention characteristics in ferroelectric-gate FETs is mainly discussed.

2. Data Retention Characteristics

The short retention time in the MF(M)IS structure is caused by a dielectric capacitor connected in series to the ferroelectric capacitor. In this structure, electric charges $\pm Q$ based on the remanent polarization of the ferroelectric film also appear on the electrodes of the dielectric capacitor (capacitance C). Since the relation $Q = CV$ is satisfied in the dielectric capacitor, the relation in the ferroelectric capacitor becomes $Q = - CV$ when the gate electrode is grounded. That is, the direction of the electric field in the ferroelectric film is opposite to that of the polarization. This depolariza- tion field reduces the data retention time significantly [1].

In order to make the depolarization field low, C must be as large as possible. That is, a thin buffer layer with a high dielectric constant is desirable. It is also desirable in the MFMIS structure that the area of the MIS part becomes larger than that of the MFM part. Another important point is to reduce the leakage current of both ferroelectric and dielectric films, so that the charge neutrality at a node between the two capacitors is not destroyed.

3. Characteristics of Ferroelectric-gate FETs

Effectiveness of the MFMIS gate structure was first demonstrated by Nakamura et al. [2], in which p-channel FETs with an $Ir/IrO_2/PZT(PbZr_{1-X}Ti_XO_3)/Ir/IrO_2/poly\text{-}Si/SiO_2/Si$ gate structure was fabricated. In their I_D-V_G (drain current vs. gate voltage) characteristics, the memory window (threshold voltage shift) of 3.3V and a current on/off ratio of 6 orders-of-magnitude were obtained for voltage sweep of ±15V. It was also demonstrated in the FETs with a $Pt/SBT\ (SrBi_2Ta_2O_9)/Pt/SiO_2/Si$ gate structure that the data retention characteristics were much improved by increasing the gate MIS area, compared to the MFM capacitor area [3].

However, high-density integration of the MFMIS-FET is difficult, because the gate MIS area must be designed much larger than the MFM capacitor area. Thus, studies on MFIS-FETs with high-k dielectric buffer layers became important. Typical high-k materials are Si_3N_4 [4], Al_2O_3, HfAlO[5], HfO_2 [6], $LaAlO_3$[7] and so on.

Sakai et al.[5] demonstrated that the on- and off-currents in MFIS-FETs with a HfAlO buffer layer and an SBT ferro- electric film were clearly distinguishable for at least 12 days. More recently, we also demonstrated that the data retention time of FETs with a $Pt/SBT/HfO_2/Si$ gate structure was longer than 30 days [6]. Another approach is to use a low-k ferroelectric film. Li et al. demonstrated 4-day data retention using $Pb_5Ge_3O_{11}$ [8]. We conclude from these recent results that use of high-k dielectric buffer layers and/or low-k ferro- electric films is promising for fabricating ferroelectric-gate FETs with excellent data retention characteristics.

4. 1T2C-type Nondestructive Readout Cell

In an MF(M)IS-FET it is very difficult to retain data for 10 years, because they are easily destroyed by the gate leakage current based on the depolarization field. In order to solve this problem, a novel cell, in which two ferroelectric capacitors with the same area are connected to the gate of a MOSFET, has been proposed [9]. In this cell two ferro- electric capacitors are polarized oppositely with respect to the gate electrode, so that the electric charges on the electrodes of both capacitors are canceled each other and no charge is induced to the gate electrode. Under this condition, no depolarization field is generated in the ferroelectric film.

In the readout operation, voltage pulses are applied to one terminal, keeping the other terminal open. In this operation, when the stored datum is "0", no polarization reversal occurs in the ferroelectric film and a little drain current flows through the MOSFET and vice versa. Non-destructive readout and long data retention characteristics have been demonstrated in this cell [10]. The cell is also suitable for high-density integration, because it can be shrunk according to the scaling rule.

5. Summary

Recent progress in FET-type ferroelectric memories is reviewed. Since the retention characteristics of ferroelectric- gate FETs have been much improved, applications to various SOC (system-on-a-chip) circuits are expected, as well as those to high-density stand-alone memories.

Reference

1) H.Ishiwara; Mat. Res. Soc. Symp. Proc. **748**, 297 (2003)
2) T.Nakamura, Y.Nakao, A.Kamisawa, and H.Takasu; Integrated Ferroelectrics, **9**, 179 (1995)
3) S-M.Yoon, E.Tokumitsu, and H.Ishiwara; Jpn. J. Appl. Phys. **39**, 2119 (2000)
4) K-H.Kim, J-P.Han, S-W.Jung, and T-P.Ma; IEEE Electron Device Lett. **23**, 82 (2002)
5) S.Sakai and R.Ilangovan; IEEE Electron Device Lett. (in press)
6) K.Aizawa, K.Takahashi, B-E.Park, and H.Ishiwara; (unpublished)
7) B-E. Park and H. Ishiwara, Integrated Ferroelectrics, **52**, 187 (2003)
8) T.Li, S.T.Hsu, B.D.Ulrich, L.Stecker, D.R.Evans and J.J.Lee; IEEE Electron Device Lett. **23**, 339 (2002)
9) H.Ishiwara; Integrated Ferroelectrics, **34**, 11 (2001)
10) S-M.Yoon and H.Ishiwara; IEEE Trans. **ED-48**, 2002 (2001)