Abs. 874, 206th Meeting, © 2004 The Electrochemical Society, Inc.

RELIABILITY CHALLENGES FOR SUB-90NM TECHNOLOGY DIELECTRICS

H. Puchner
Cypress Semiconductor, Technology R&D
3901 N. First Street, San Jose, CA95134
Tel: 408-232-4514; Fax: 408-232-4417; E-mail:
hrp@cypress.com

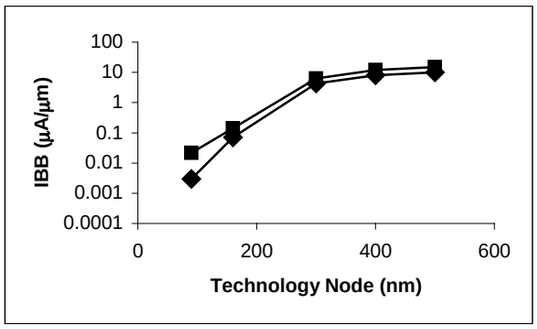
We present a comprehensive review of reliability challenges for gate dielectrics down to the 65nm technology node. The major reliability degradation mechanisms are analyzed for CMOS technologies. Historical data will show that hot carrier degradation has lost on importance and that negative bias temperature instability (NBTI) is the leading reliability concern for the 65nm technology node. Additionally, dielectric breakdown as well as gate leakage currents pose an important limitation to the maximum applicable voltage across the gate oxide. The recent trend of overdriving transistors by applying a higher gate electric field has caused serious concerns with regards to dielectric reliability. Finally, we are discussing the overall chip level reliability concerns and design methodologies needed to comprehend gate oxide reliability.

The gate dielectric has been the subject of constant improvement and innovation since the invention of the MOSFET transistor. The gate oxide is the major transistor component to control the transistor channel underneath with respect to leakage currents as well as saturation drive currents. The demand for higher drive currents and better performance has also pushed the gate oxide thickness towards it material limits, especially as we enter the 65nm technology node. The common candidate for the ultimate gate dielectric, silicon dioxide, is facing its structural boundaries and silicon dioxide/nitride stacks will become mainstream for 65nm technologies and beyond. The medium dielectric k-number of nitride allows thicker physical oxides to control direct tunneling currents. However, the ultimate dielectrics are high k-number gate materials such as hafnium oxide or zirconium oxide. Both dielectric materials have still not demonstrated comparable carrier mobilities as well as dielectric integrity and reliability. In addition, high-k dielectrics suffer from severe charge trapping effects reducing the reliability drastically as well as new breakdown phenomena never experienced before with silicon dioxide based gate oxides.

Since today's products operate at elevated temperatures product level reliability at temperature is becoming increasingly important. Typical HTOL "Hot Temperature Operating Life" tests are common in the industry. During HTOL testing the product is brought up to elevated temperature and the devices are toggled or tested with a certain product speed at accelerated supplies. Previously, only gate oxide reliability as well as hot carrier reliability was of concern. Now NBTI adds an significant impact on the overall lifetest. It is important to be able to simulate the impact of NBTI on a circuit level using SPICE simulators. The above described NBTI model can be implemented as procedural function call during the netlist extraction sequence. The procedural interface needs also the cycling information from circuit simulations (Verilog level). Each transistor model can be changed individually by adjusting the threshold voltage in the SPICE model. Alternatively, all transistor corners might be shifted together as a worst case estimate. Compared to HCI reliability it is difficult to identify NBTI critical circuitry. However, DC biased circuits are more prone to NBTI degradation and need to be identified as early as possible in the design cycle.

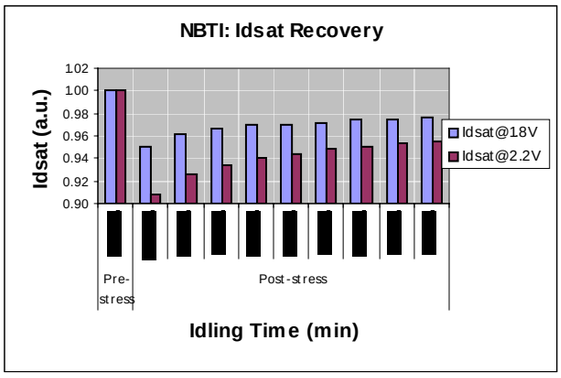
We will present a comprehensive analysis of the major reliability concerns for deep sub-micron technologies. HCI reliability has become less of a concern for state-of-the-art technologies, where NBTI has risen to the major reliability challenge. We present an analytical NBTI model, which can be easily implemented into a spice modeling engine and which considers all possible aspects. Depending on the bias conditions, temperature, and duty cycling a certain absolute threshold voltage shift was extracted. The same models could be constructed for drive current degradation or linear threshold voltage degradation. This model allows the design community to estimate the impact of NBTI on their product performance. TDDB reliability generally improves with the level of nitrogen in the gate dielectric, however the recent trend of overdriving the gate oxides with higher gate voltages has a severe impact on TDDB reliability.

HCI Reliability



Substrate current for different technology nodes

NBTI Recovery



Drive current recovery after NBTI stress