

Assessment of 3D for Future On-Chip Wiring and Novel System Solutions

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In the semiconductor industry the world of 3D has two faces. On one side, 3D is associated with the backend of line (BEOL) in future MPUs and considered as a novel interconnection scheme which might be necessary when following Moore's law by downscaling of existing high performance logic products; the so-called "red brick walls" in the interconnect chapter of the International Technology Roadmap for Semiconductors (ITRS, /1/) have given rise to discussions for a search for new on-chip interconnect schemes to avoid the "interconnect crisis". 3D as a potential novel BEOL approach means to replace today's metallization schemes featuring up to 9 levels of metal on top of a single device layer by stacking and vertically interconnecting several (rather similar) device layers, each of which having only a few metal layers; one can imagine that within the individual device layers in the stack the interconnections could then even be achieved with relaxed requirements regarding design layout and unit processes; thus the global interconnects, the longest interconnections across a chip, could be kept shorter than with today's state-of-the-art approach with many levels of metal on a single device layer. Such an approach is characterized by roughly requiring the same total area A of silicon as conventional technology, while featuring a reduced footprint (A/n) in the stack of n device layers. It has been reported /2/ that stacking of 5 device layers may result in almost half the RC delay.

Beyond this BEOL related 3D architecture, optical and RF/ μ -wave based signal transport have been discussed as potential on-chip interconnect solutions for future chip wiring /1/. For the BEOL the main application in mind is clock distribution. This is the second face of 3D, namely the stacking and vertical interconnection of (rather dissimilar) technologies. Regarding optical on-chip interconnects based on III-V materials, the disparity of the technologies, component sizes, CDs, the supply voltages, and in particular the high operating temperature ($T_{use}=105^{\circ}\text{C}$) in the silicon world are the obstacles for 3D of Si and III-V. RF/ μ wave-based clock distribution may but must not necessarily utilize 3D. Applying the Raleigh criterion for on-chip antennas requires transmitter-receiver distances comparable with chip extensions and thus an application of this technique to chip-to-chip data transfer rather than an on-chip LAN; further concerns are associated with the component size of waveguides, cross-talk and noise.

Recent investigations /3/ on the various aspects of deep sub-100nm Cu-based interconnects fabricated with standard manufacturing lithography (and a trick) will be discussed. The results show that some "red brick walls" even for end-of-roadmap chip generations are getting cracks and that in the 14 years ahead until the end of the current edition of the ITRS the "no known solutions" can be turned into "solutions known". The results also show that conductor resistivity ($\rho_{Cu}=2.2\mu\Omega\text{cm}$) is remaining rated "no known solution". Future interconnect schemes will, however, rather probably be evolutionary rather than revolutionary if close concurrent development of design and technology will be practiced. Design has not yet been driven to its limits as has been the case with technology. Encouraging examples for this assessment are the recent advances of design realizing hardware with X-architecture /4/ for on-chip wiring. Furthermore an estimation shows that if design can keep local interconnects short ($<20F$), local interconnects might be embedded in SiO_2 as

intermetal dielectric even for 45nm node products without being primarily compromised by wire related RC signal delay.

The motivation for the 3D approach which is not related to BEOL on-chip wiring is to come up with new products and new systems. SOC is one of the keywords. Various 3D concepts and stacking techniques have been discussed /5/ for many years as enabling technologies for new systems and have made progress.

3D products where the stacking is done in the backend (BE) to save chip packages and board area have been in production /6/ since years. 3D efforts with stacking in the BEOL to fabricate new systems, beyond these packaging cost and board area driven applications, are remaining under investigation and development with focus on improvement of reliability and/or yield. A first product is in sight /7/. When once, more will be demonstrated than the proof of principle, the fascinating technology of 3D has the potential to become the enabler for cost effective manufacturing of embedded system solutions (SOC)

The key unit processes for thinning, gluing/bonding and vertical interconnection required for both variants of 3D remain challenging. For both the BEOL and the SOC variant of 3D, wafer-to-wafer, chip-to-wafer, and chip-to-chip stacking are conceivable and exhibiting the trade-off between performance and throughput. Fabrication costs will finally decide the stacking scenario of choice for each future 3D semiconductor product to come.

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References

- /1/ 2003 Edition of the ITRS, <http://public.itrs.net/>
- /2/ P. Kapur et al, SEMICON West 2002, SEMI Technical Symposium (STS), Semiconductor Equipment and Materials International, p. 159 (2002)
- /3/ M. Engelhardt et al, MICRO.tec 2003 Proc. Vol. , p. 259 (2003), Munich, Germany, and references therein
- /4/ www.techonline.com/community/news/14441, www.golem.de/0402/29811.html
- /5/ CD of the International Workshop on 3D System Integration, Dec. 16, 2003 at the Fraunhofer Institute, IZM, Munich, Germany
- /6/ www.amkor.com, www.irvine-sensors.com
- /7/ H. Hübner in /5/