TECHNOLOGY AND APPLICATIONS OF THREE-DIMENSIONAL INTEGRATION

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ABSTRACT

Three-dimensional (3-D) integration holds tremendous potential to reduce global interconnect latency and power dissipation, and to improve integrated circuits (ICs) form factor. Moreover, it allows heterogeneous integration of different functional blocks (e.g., logic, memory, RF, etc) and materials (e.g., Silicon, SiGe, III-IV, etc). This paper explores the opportunities and challenges of a 3-D integration approach based on a silicon layer transfer process. It combines low temperature direct wafer bonding (Cu-to-Cu and SiO_2-to-SiO_2), high rate and selectivity silicon etching, and wafer de-bonding. A thorough description of process integration will be given and key technological challenges will be highlighted. In addition, CAD tools for 3-D ICs design and layout are being developed. Potential 3-D applications for system-on-a-chip (SoC) and related issues will be discussed.