Manufacturing Solutions for Developing Processes and Tools for CVD/ALD of Dielectrics for Nanoelectronics

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The most important issue currently faced by the semiconductor industry is sustaining profitability (1-2). In this paper we have described a novel method of thermal processing and CVD techniques with a focus on addressing the issues of manufacturing of high-κ dielectrics for sub-100nm CMOS and also reducing the cost associated with the process and also improve yield.

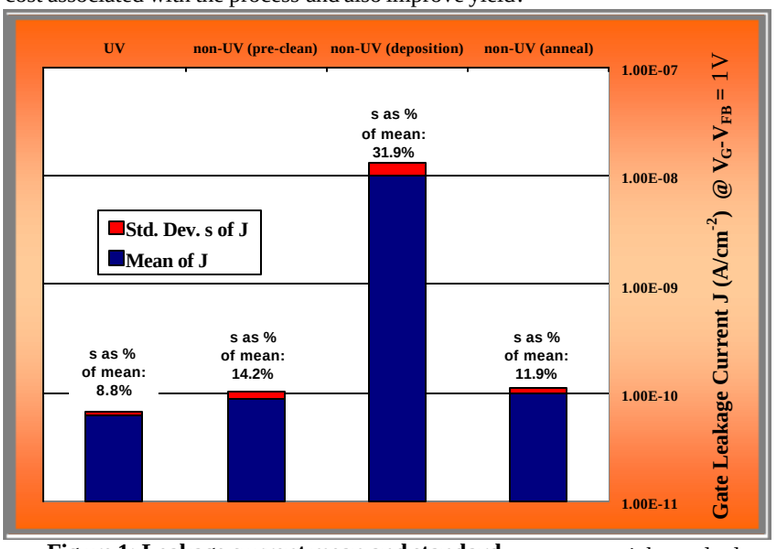

Figure 1: Leakage current mean and standard deviation for various processing conditions

We have attempted to combine the advantages of in-situ rapid thermal processing (RTP) (3-6) along with UV and VUV radiation (7) in a single wafer processing (SWP) (8-10) environment to provide for tight process control, low thermal budget, low levels of microscopic defects and consequently better device reliability. At Clemson University, we have invented a process with a lesser process variation than corresponding RTP or CVD system under a SWP type processing scheme (11).

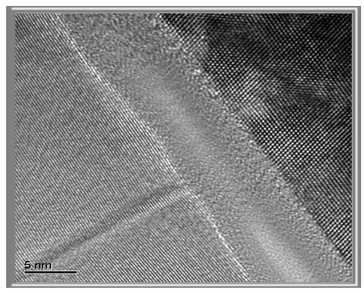

Figure 2: TEM micrograph of sample processed with UV/VUV for all steps

Results from a UV/VUV assisted MOCVD system used to deposit Al_2O_3 as a gate dielectric are presented. Wafers are pre-cleaned ex-situ using dilute HF to etch away any oxide. This is followed by an in-situ wafer clean under a forming gas atmosphere. RTP assisted CVD of Al_2O_3 is carried out using Tri-methyl Aluminum (TMA) as the precursor. The precursor exposure was followed by an oxidizing exposure with O_2 as the oxidizer. This step of alternate exposure to TMA and O_2 was done repeatedly to get better uniformity. This was followed by in-situ annealing and then by in-situ vapor deposition of Aluminum for the gate electrode. Ex-situ patterning by lithography was performed as the final processing step for the metal-insulator-substrate (MIS) structure, before electrical characterization. The same process was performed under different conditions of UV/VUV. The mean values for the gate leakage current at an effective gate bias of 1 V and capacitance were 6.24×10^{-11} A/cm^2 and 2.10 μF/cm^2 respectively for those samples which were exposed to the effect of UV/VUV during all the in-situ steps. Also, the effect of process variation was greatly reduced when UV/VUV was in place during the deposition. Leakage current standard deviation was at 8.8% of the mean and that of capacitance was 4.7%. Wafers which were subject to selective UV/VUV treatments showed poorer performance (Fig. 1). From the high resolution transmission electron microscopy (TEM) micrograph, we can observe the silicon substrate on the left of the figure (Fig. 2), followed by the Al_2O_3 insulating layer and the aluminum contact layer. It can be clearly seen, that the Al_2O_3 insulating layer is amorphous on top of the silicon substrate, and that the structure is stable without any indication for recrystallization in the Al_2O_3 layer during processing.

In conclusion, we have shown a novel method to manufacture gate dielectrics for sub-100nm CMOS with the objective of minimizing the cost associated and at the same time with no compromise on yield. The process has proven to be inherently less prone to variation, and hence it is our belief that the cost of manufacturing using this process will result in significant reduction in overall expense.

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