MICROSTRUCTURE EVOLUTION AND BREAKDOWN MECHANISM STUDIES IN MOSFET WITH ULTRA THIN GATE DIELECTRICS IN NANOMETER TECHNOLOGY ERA

Chih Yuan Lu
Macronix International Co., Ltd. Hsinchu, Taiwan, ROC
Chih Hang Tung
Institute of Microelectronics, Singapore
Kin Leong Pey
Nanyang Technological University, Singapore

Ultra thin gate dielectric breakdown and failure mechanism are studied by using transmission electron microscopy. Two new failure mechanisms, dielectric breakdown induced metal migration (DBIM) and dielectric breakdown induced epitaxy (DBIE), are reported. DBIE is confirmed to be the intermediate stage between soft breakdown and hard breakdown. Detailed physical model is proposed to explain the DBIE grow during dielectric breakdown transient.

It is observed that in all the hard breakdown and some of the soft breakdown cases, the MOSFET gate structure was damaged and the degree of destruction depends on the energy pumped into the device during breakdown event (1). Fig 1 summarizes this statement. Among the physical changes observed experimentally, DBIE is believed to be the failure mechanism that is of critical importance in understanding the gate oxide breakdown. DBIE is stress polarity dependent (2). In all the cases observed, DBIE always grows from the cathode side of the stress electrode. Fig 2 shows the TEM micrograph and the corresponding stress configuration. It is believed that during the DBIE, the nucleation of the epitaxial Si starts either at the poly-Si grain/gate oxide interface or the gate oxide/Si substrate interface where the percolation path of the gate oxide breakdown terminates, depending on the stress polarity (3). High resolution TEM lattice imaging analysis had confirmed that the epitaxial hillock is indeed an extension of the crystal from the Si substrate (Fig. 2b) or the poly-Si grains (Fig. 2a). Unlike the HBD in ultrathin SiON and Si_3N_4 gate dielectrics, in which there is always a clear DBIE formation at the BD spot, HBD DBIE formation in HfO_2 gate dielectric devices is less prominent and may have involved Hf silicide or silicate formation, as shown in Fig. 3. DBIE may have occurred but HfO_2 did not deform accordingly. Instead, DBIE has ruptured rather than caused localized thinning or bending of the gate dielectric. This indicates that the BD phenomenon in HfO_2 is different from that of the ultrathin SiON and Si_3N_4 gate dielectrics (4,5).

It was demonstrated in this study that gate dielectric breakdown in MOSFET devices involve destruction processes that go beyond the dielectric layer itself. Both polysilicon and Si substrate play an active and even dominant role in determining the breakdown transient process and thus the post breakdown device electrical characteristics.

References

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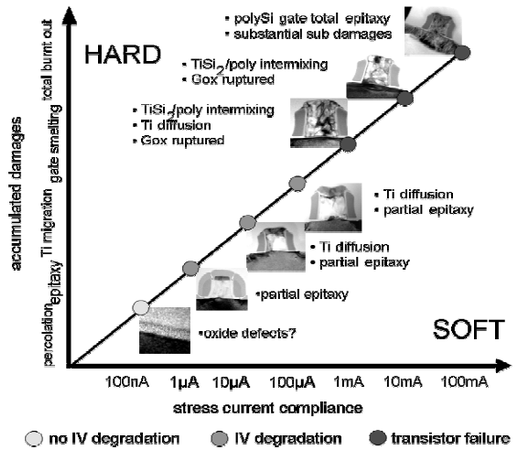

Fig 1 A summary on the relationship between physical damages generated by a gate oxide breakdown and the corresponding compliant current levels under a constant voltage stress (CVS) condition (1).

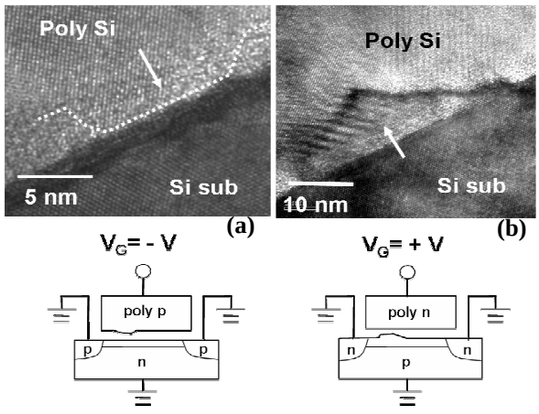

Figure 2 Cross sectional TEM micrographs of a poly-Si gate structure showing damages at various compliance current levels (a) 100nA of a Co-silicided 25Å gate oxide pMOSFET and (b) 1μA of a Co-silicided 25Å gate oxide nMOSFET. Si epitaxial extrusion indicated by the arrow from (a) poly Si and (b) Si substrate into the gate oxide is observed in both samples. The stress voltage was set at 4.4V. The arrows indicate the Si epitaxy (2).

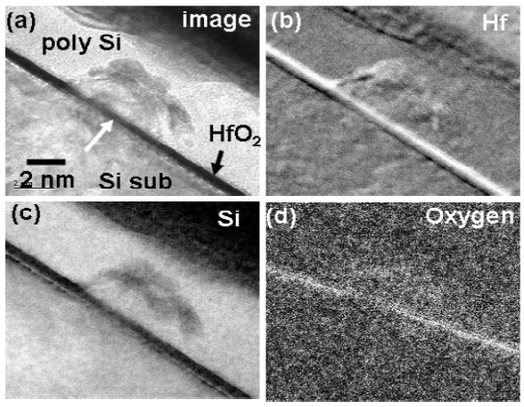

Figure 3 Cross section TEM on post hard breakdown nMOSFET device with HfO_2 gate dielectric, (a) bright field TEM image showing the breakdown spot (indicated by white arrow), EELS mapping with (b) Hf, (c) Si, and (d) oxygen (3).