TOWARDS 0.5 nm EOT SCALING OF HfO_2 / METAL ELECTRODE GATE STACKS

Jeff J. Peterson, George A. Brown, Ken Matthews, Jim Gutt, Sundar Gopalan, Hong-Jyh Li [a], Paul Kirsch [b], Joel Barnett, Naim Moumen [b], Craig Huffman [c], Prashant Majhi [d], Nirmal Chaudhary [a], Chadwin D. Young, Barry Sassman, Byoung-Hun Lee [b], Gennadi Bersuker, Peter M. Zeitzoff, Pat Lysaght, Mark Gardner [e], Robert W. Murto [c], and Howard R. Huff

International SEMATECH, 2706 Montopolis Dr., Austin, TX 78741

Assignments from: [a] Infineon, [b] IBM, [c] Texas Instruments, [d] Phillips, and [e] AMD

ABSTRACT

The International Technology Roadmap for Semiconductors (ITRS) projects that future high performance processes will require transistor gate stacks having equivalent oxide thickness (EOT) of 0.6 nm in the next decade [1]. Since the gate stacks of future processes will likely consist of bottom interface (BI), high-k dielectric, and metal gate electrode layers, an important step in scaling the EOT of the composite gate stack is to understand the relative EOT contribution and scaling limitations for each layer. Previous investigations show the substrate/BI layer is critical for carrier mobility and EOT scaling of high-k gate stacks [2], [3]. Likewise, scaling of the high-k dielectric layer requires optimization of the deposition process to address growth initiation and coverage concerns [4]. The use of metal gate electrodes in high-k gate stacks is also known to be favorable to EOT reduction since it eliminates polysilicon (poly-Si) depletion during transistor inversion [5] and restricts EOT increase due to top interfacial reactions between the high-k dielectric and the poly-Si gate electrode [6].

Furthermore, transistors incorporating sub-0.6 nm gate stacks must demonstrate good transistor characteristics after 1000ºC or greater rapid thermal anneal. It is well known that high-k transistor transconductance (G_m) and I_{on} drive currents are greatly affected by the mobility, which is affected by the BI layer quality and physical thickness [2]. The use of HfO_2 high-k dielectric with poly-Si gate electrodes is known to result in transistor flat band (V_{fb}) and voltage threshold (VT) shifts, likely a result of Fermi level pinning [7], signaling the likely use of dual metal gates to provide the proper transistor VT. Lastly, the ability of sub 1.0 nm gate stacks to maintain good transistor characteristics subsequent to the 1000ºC source/drain (S/D) activation anneal places a heavy constraint on the gate stack materials to inhibit interfacial and bulk reactions within the gate stack.

This paper presents results of significantly scaled high-k transistor gate stacks through:

(i) reduction of the BI layer using an HF-last/NH_3 anneal interface,
(ii) significant thickness reduction of the HfO_2 dielectric, and
(iii) use of TiN-poly-Si metal gate electrodes.

Using these deeply scaled gate stacks we discuss scaling trends of high-k transistors as well as the implications that these sub-0.6 nm EOT gate stacks hold for the semiconductor roadmap.

REFERENCES

[1] Semiconductor Industry Association (SIA), International Technology Roadmap for Semiconductors (ITRS), 2003 Edition, Austin, TX: International SEMATECH, 2003. (This is available for viewing and printing at URL: http://public.itrs.net)

[2] E. P. Gusev, D. A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P.C. Jamison, D. A. Neumayer, M. Copel, M. A. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L. A. Ragnarsson, P. Ronsheim, K. Rim, R. J. Fleming, A. Mocuta and A. Ajmera, "Ultrathin high-k gate stacks for advanced CMOS devices", IEDM Conf. Proc., p. 451, 2001.

[3] Massimo V. Fischetti, Deborah A. Neumayer, and Eduard A. Cartier, **"**Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-k insulator: The role of remote phonon scattering", J. App. Phys., **90**, p. 4587 (2001).

[4] G. D. Wilk, Dave Muller, Jan Willem Maes, "Recent Developments in Understanding Local Effects and Device Properties of Hf-based High-k Dielectrics", 2004 MRS Spring Meeting Abstracts, San Francisco, CA (2004), p. 84.

[5] Howard Huff, A. Hou, C. Lim, Y. Kim, J. Barnett, G. Bersuker, G. Brown, C. D. Young, P. Zeitzoff, J. Gutt, "High-k gate stacks for planar, scaled CMOS integrated circuits", Microelectronic Engineering, **69**, p. 152 (2003).

[6] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations**"**, J. App. hys., **89**, 10, p. 5243 (2001).

[7] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, P. Tobin, "Fermi level pinning at the polySi/metal oxide interface**"**, VLSI Conf. Proc., p. 9, 2003.