Electrical conduction processes in Lanthana thin films prepared by E-Beam Evaporation

Yongshik Kim, Shun-ichiro Ohmi, Kazuo Tsutsui, and Hiroshi Iwai

Tokyo Institute of Technology
4259 Nagatsuta, Midori-ku, Yokohama 226-8502, Japan
Phone: +81-45-924-5174, Fax: +81-45-924-5174
E-mail: yskim@ae.titech.ac.jp

Abstract

Lanthana (La_2O_3) films were deposited by E-beam evaporation on n-Si (100). For the sake of comparison, some films were annealed in an *ex-situ* way at different temperatures with nitrogen gas flow for 5 min. From current-voltage measurement of the as-deposited films, ultra low gate oxide leakage current is observed while some films show variation in the scale of the currents. It is shown that all the currents of as-deposited films obey the same conduction mechanisms irrelevant of the leakage current scale. From the electric field and temperature dependence of the current of the gate oxide, it is shown that the main conduction mechanism is the SCLC (Space-Charge-Limited Current) at low oxide field region and F-N (Fowler-Nordheim) conduction at high oxide field region. It is also shown that conduction processes verified at the as-deposited films is again observed at the nitrogen annealed films.

Introduction

Lanthana thin film is being focused for the gate dielectrics of MOSFET in the next generation due to ultra-low leakage currents [1]. In this paper, we report the result of detailed analysis in the conduction mechanisms of the as-deposited Lanthana films compared to *ex-situ* annealed films with nitrogen gas flow.

Experiments

Lanthana thin films were deposited on HF dipped n-Si(100) substrate by E-beam evaporation at 250°C. The pressure in the chamber during depositions was around 10^{-9} Torr. Then, some films were annealed in the RTA (Rapid Thermal Annealing) chamber with a controlled flow of oxygen or nitrogen gas. After PDA (post-deposition anneal), gate electrode was formed by metal evaporation with a shadow mask using bell-jar type evaporator at around 10^{-5} Torr.

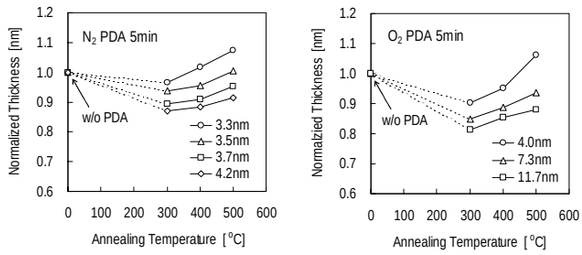
Results

Figure 1 shows change in film thickness with PDAs. Increase in thickness indicates interfacial layer growth. Figure 2 shows inverse of capacitance with film thicknesses. Intercept of fitted lines to vertical axis at zero film thickness is found to be non-zero, which describes interfacial layer thickness. This is in agreement with the results depicted in Figure 1.

Figure 3(a) shows gate leakage currents as a function of gate voltage with a variation in the currents. Leakage currents were found to be associated mainly with SCLC and F-N as shown in Fig.3(b). Figure 4 shows leakage currents for a film with nitrogen PDA. It is found that conduction models are qualitatively same between as-deposited and nitrogen annealed films.

Conclusions

The conduction process of the as-deposited and nitrogen-annealed Lanthana thin films were analyzed and compared. The conduction is caused by the SCLC at the low oxide field region and the F-N current at the high field region. Variation in the scale of the leakage currents at low oxide field is thought to be due to an amount of traps incorporated during deposition and/or annealing.



(a) nitrogen ambient (b) oxygen ambient

Fig.1. Normalized film thickness as a function of annealing temperatures for nitrogen and oxygen PDAs. Film thicknesses measured using spectroscopic ellipsometry were normalized with respect to that of as-deposited film.

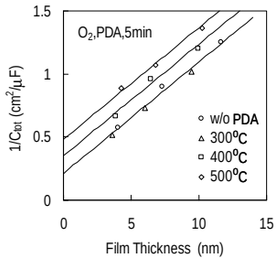
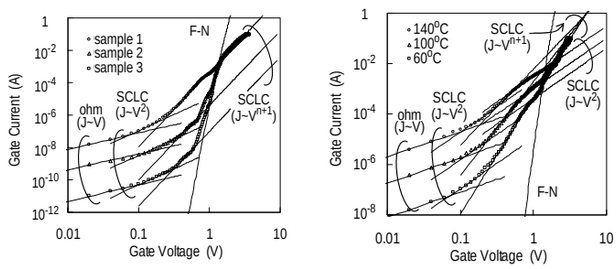


Fig. 2. Inverse of the accumulation capacitance $1/C_{tot}$ as a function of the optical film thickness of Lanthana without and with different oxygen PDAs. Solid lines are fits to the experimental results.



(a) leakage currents for three samples at 60°C (b) leakage currents for sample 1 of (a) at different temperatures.

Fig. 3. Gate leakage current of 4 nm film of Al gate electrode, as a function of gate voltage. Annealing after deposition was not carried out. Solid lines are the best fits to experimental results. Conduction models and current-voltage relation are described near the fitted lines. Gate area is $3.14 \times 10^{-4} cm^2$. Symbols correspond to experimental results of (a) three samples showing variation in the currents at 60°C and (b) one sample marked with 1 in (a) at different measurement temperatures. Power term n of gate voltage of (a) is 3.6 for three samples. n powers in (b) are 3.6, 2.7, and 2.0 at 60, 100, and 140°C measurement temperatures, respectively.

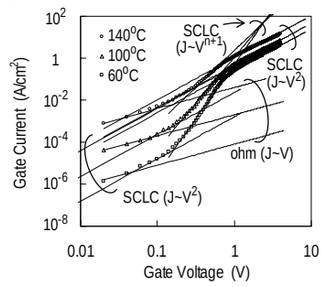


Fig. 4. Gate leakage current of 7.7 nm film of Pt gate electrode, as a function of gate voltage. The film was annealed with 400°C nitrogen PDA for 5 mins. Symbols correspond to experimental results of different measurement temperatures. Solid lines are the best fits to experimental results. Conduction models and current-voltage relation are described near the fitted lines.

Acknowledgements

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Reference

[1] Y.Yeo, T.King, and C.Hu, Appl.Phys.Lett., 81(11), 2091-93 (2002).