Novel TFTs for Large Area Electronics

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Microelectronics and, particularly, silicon integrated circuit microelectronics, has produced amazing capabilities over the last 40 years. There are numerous indicators of this, but best summarized as "Moore's Law." While more transistors/ cm^2 is the driving force, the microelectronics-based display industry has, for over a decade also explored alternate directions – larger and larger "chips" and/or alternative substrates. Thus, displays have grown from several in^2 to several ft^2 while the number of transisors/cm^2 has remained small. Further, major R & D investment has been made in migrating from a glass substrate "chip" to a plastic one in order to achieve increased functionality (again without increasing the transistors/ cm^2).

The relatively low cost manufacturing process used for displays has created significant interest in applying this form of microelectronics to other classes of problems. An example is an image sensor array. Other sensor techniques would provide the capability to monitor stress or corrosion while integration of actuators would lead to the capability to not just monitor the environment, but to respond to it (modification of a property in response to a stimulus).

To accomplish such sensor applications, more transistors/ cm^2 is not the issue. Rather the ability to cost effectively fabricate modest numbers of integrated devices ($<10^5$) over large areas ($>ft^2$) is essential. Even then, other attributes may also be required (such as compatible MEMS devices for integration and flexible substrates). Perhaps the most demanding feature that has not been developed by either the integrated circuit or display industries is a high performance TFT.

Transistor performance is determined by materials properties and critical dimensions. Microelectronics progress has been based on the favorable material characteristics of silicon (and its oxide) and the drastic scaling (from 10's of microns to tenths of microns) that has been achieved. Cost effective manufacture of TFTs over large areas limits both the material and dimensional properties that can be achieved and results in a 10-100x reduction in device performance. While not a significant limitation for displays, it is for applications that require performance in the MHz and higher regime.

One approach to achieving higher performance TFTs is to improve the process conditions that are currently used to fabricate poly TFTs. Improved re-crystallization methods will result in better mobility, on/off ratio, and device-to-device uniformity. Further, reduced surface roughness will yield a better quality, thinner gate oxide to reduce V_t and improve speed. Such objectives can be achieved by better recrystallization and oxidation methods or by processing "off line" and then transferring onto the preferred substrate. While such methods are well known, there are still challenging technical hurdles. A novel means to circumvent many of these problems might be accomplished via printing of multiple Si nanowires or C nanotubes as the active material of TFTs. Both materials have significant issues, which must be overcome.

A higher payoff, but significantly higher risk approach is to replace Si. Just as various 3/5 semiconductors have significant performance advantages over Si in conventional microelectronics, exploring superior materials properties could lead to major advances in TFT performance. Several material systems promise RF capabilities of > 100 GHz under ideal conditions. Even a 10-100X reduction in performance could provide devices in the 1-10GHz range. The challenges here are not just technical, but also economic. Cost is a major factor for large area systems, so it is not sufficient to only be technically viable.

DARPA is currently funding work in a variety of areas expected to impact the migration of microelectronics from "smaller is better" to "bigger is better". Status and objectives of these efforts will be presented.