Fabrication and characterization of n- and p-channel poly-Si TFTs by sputtering deposition of ultra thin gate SiO_2 films

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As the promising material for future displays, such as system on panel, low temperature poly-Si TFTs have been widely studied. In order to improve the drivability of TFT, deposition of high quality thin gate oxide is one of the key issues. In this study, we have fabricated the n- and p-channel TFTs with ultra-thin gate oxide and analyzed the circuit performance.

Crystallized poly-Si film was prepared by solid phase annealing at 600℃ for about 10 hrs. Thin gate SiO_2 films with a thickness of 9.5nm and 6.0nm were deposited by sputtering at 200℃. Figure 1 shows the transfer curves o TFT with gate oxide thickness of 9.5nm. With the decrease of gate length, an increase of drain current and a decrease of off current were observed. The output curves indicated the ideal shape, as shown in Fig.2.

Furthermore, we have analyzed n- and p-channel CMOS TFTs with gate oxide thickness of 6.0nm. As shown in Fig.3, both n- and p-channel TFTs shows good transfer curves with ON/OFF ratios of more than 7 decades. In th n-channel TFT, mobility of more than 120 cm^2/VS was obtained.

CMOS ring oscillator consisting of the TFT with the ultra thin gate oxide was measured as shown in Fig.4. Clear oscillation with frequency of more than 20MHz was observed for the supply voltage as low as 5V.

We can conclude that ultra thin gate oxide deposited by sputtering technique is one of the promising methods to prepare the TFT with high performance for the development of future displays.

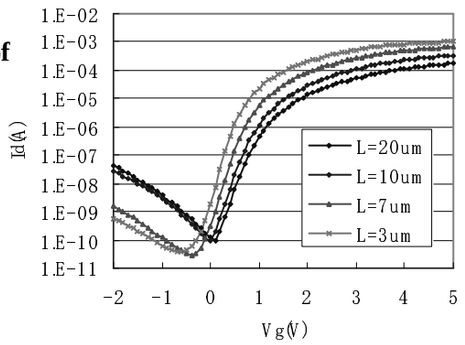

Fig.1 Transfer curves of TFTs (Tox=9.5nm).

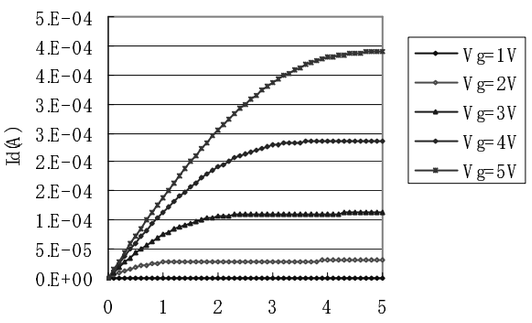

Fig.2 Output curves of TFTs (Tox=9.5nm).

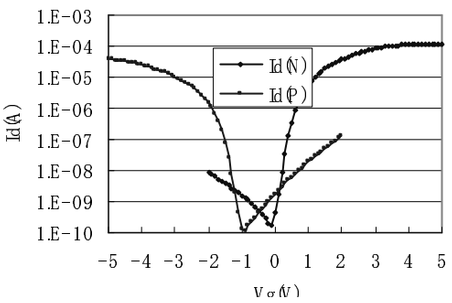

Fig.3 n-ch and p-ch TFTs (Tox=6.0nm).

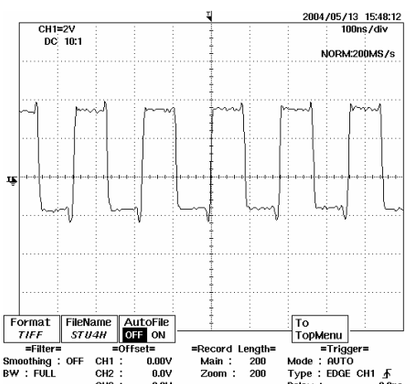

Fig.4 CMOS ring oscillator (Tox=6.0nm).